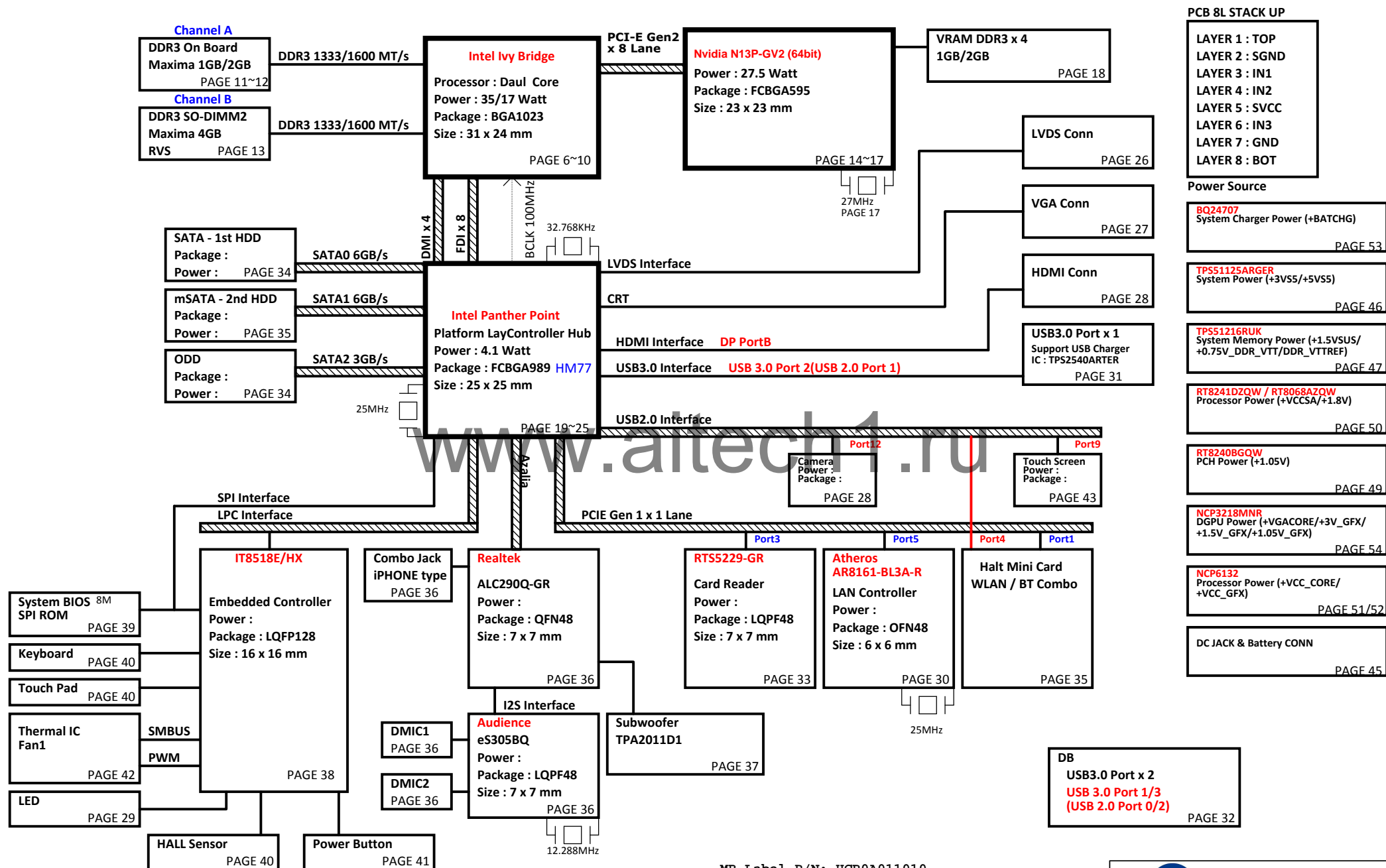
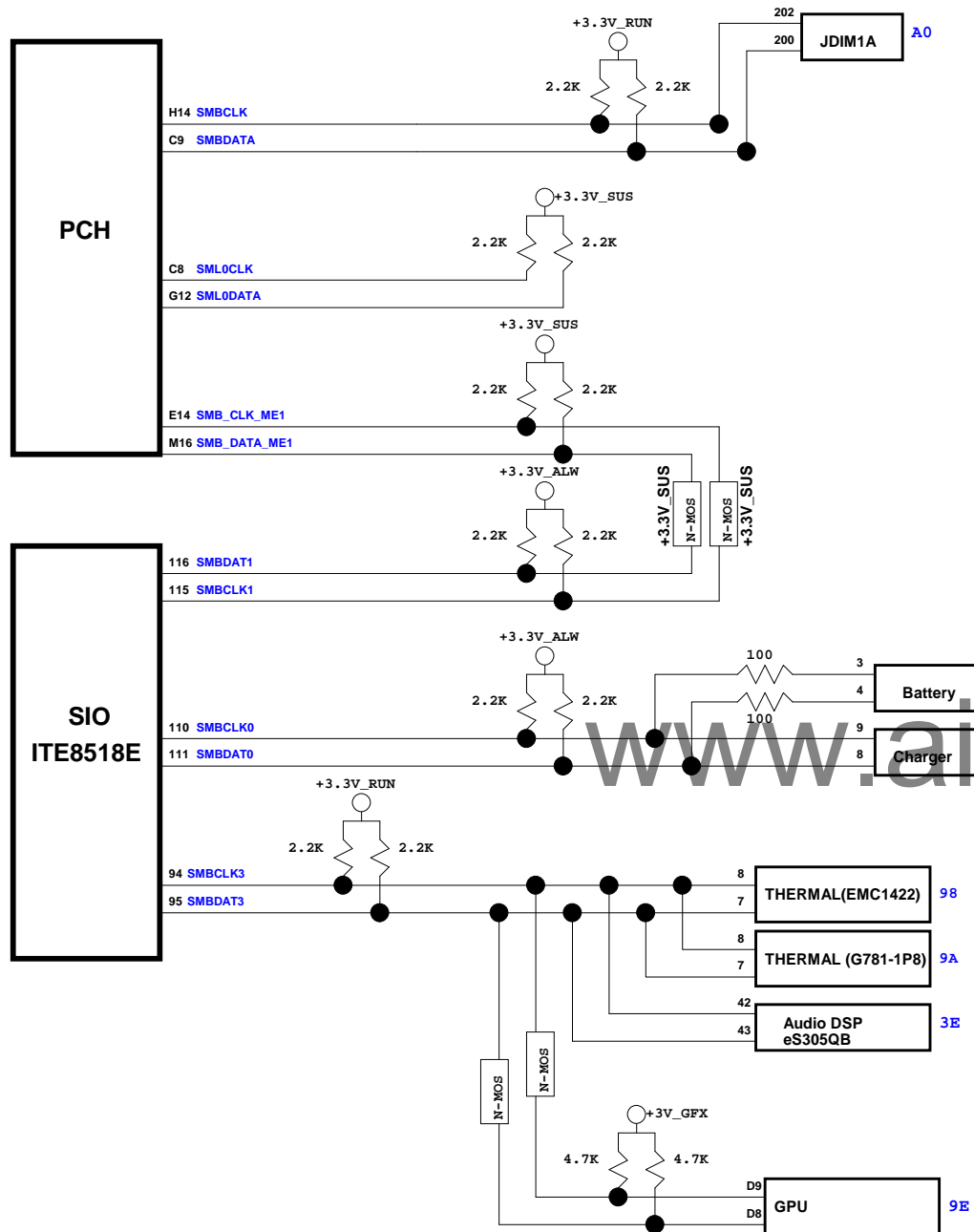


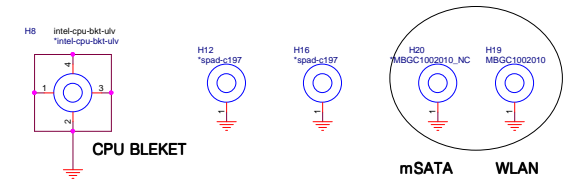
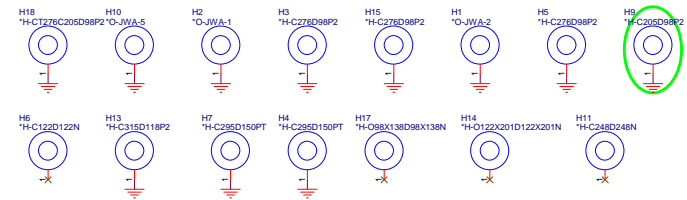
JWA 15.6" Intel Chief River Platform Block Diagram

01





SCREW PAD



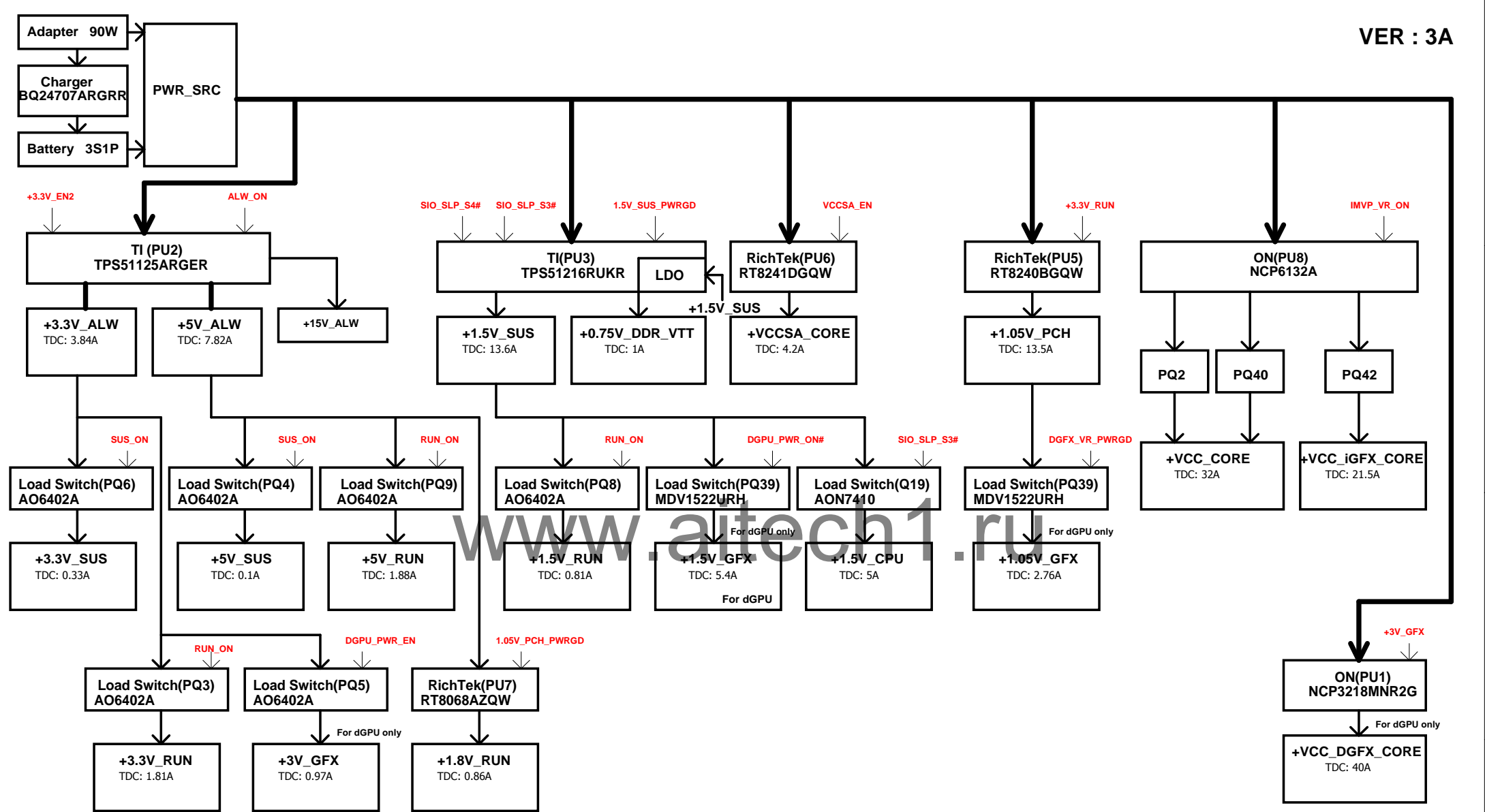
Function	IC	SMBus Address
DDR3	JDIM1A	A0h
Thermal IC	EMC1422	1001100xb (98h)
	G781-1P8	1001101xb (9Ah)
Charge IC	BQ24707ARGRR	0b0001001x (0x12h)
Battery	Battery	16h
Audio DSP	eS305QB	3Eh
GPU	N13P-GV2	9Eh

USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0 /Power share/debug port)
USB2	External port#3 (USB3.0)
USB3	NC
USB4	MiniCard 1 (WLAN/BT)
USB5	NC
USB6	NC
USB7	NC
USB8	NC
USB9	Touch panel
USB10	NC
USB11	NC
USB12	Camera
USB13	NC

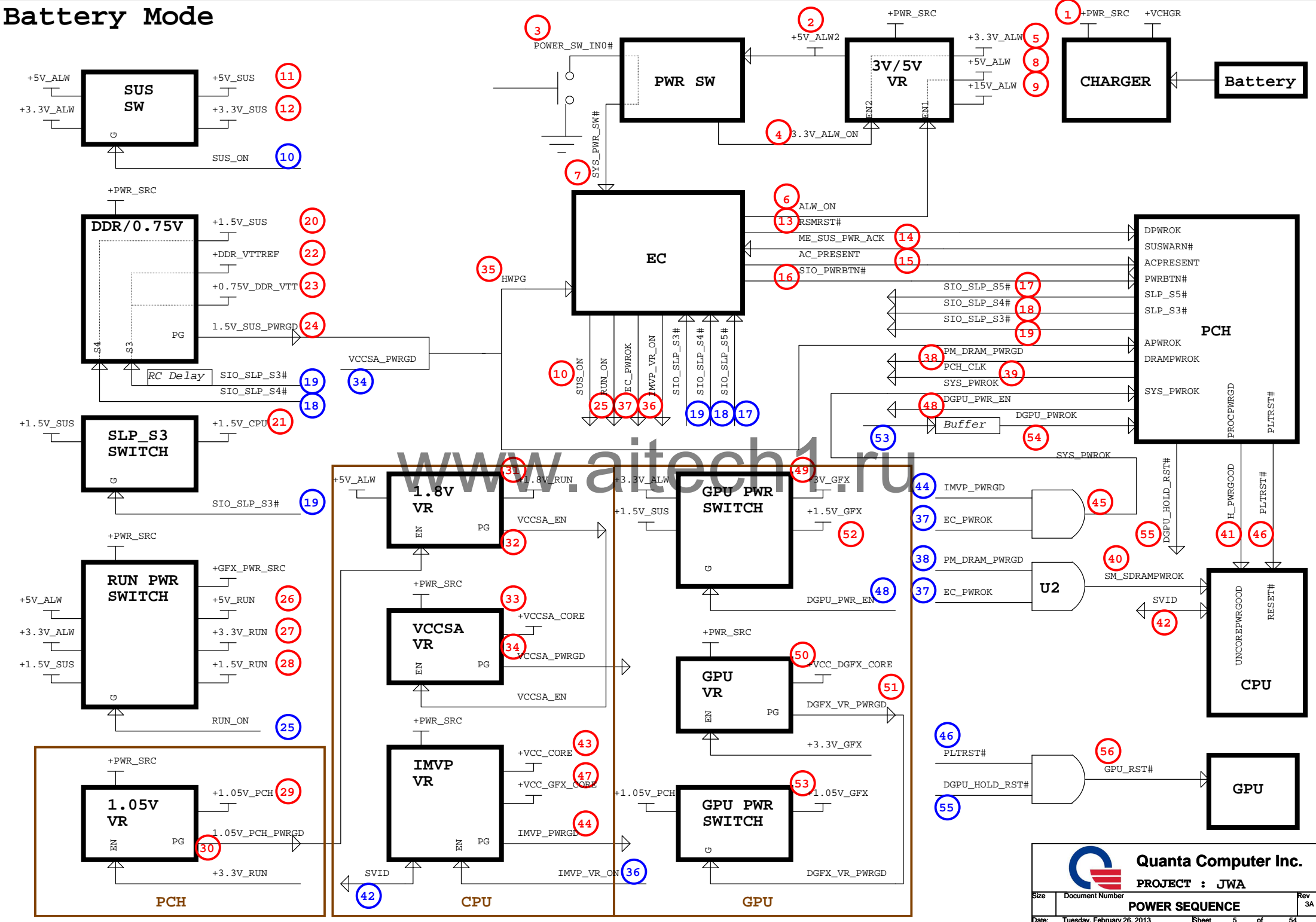
SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	NC
PCIE 3	Card reader
PCIE 4	NC
PCIE 5	LAN
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC

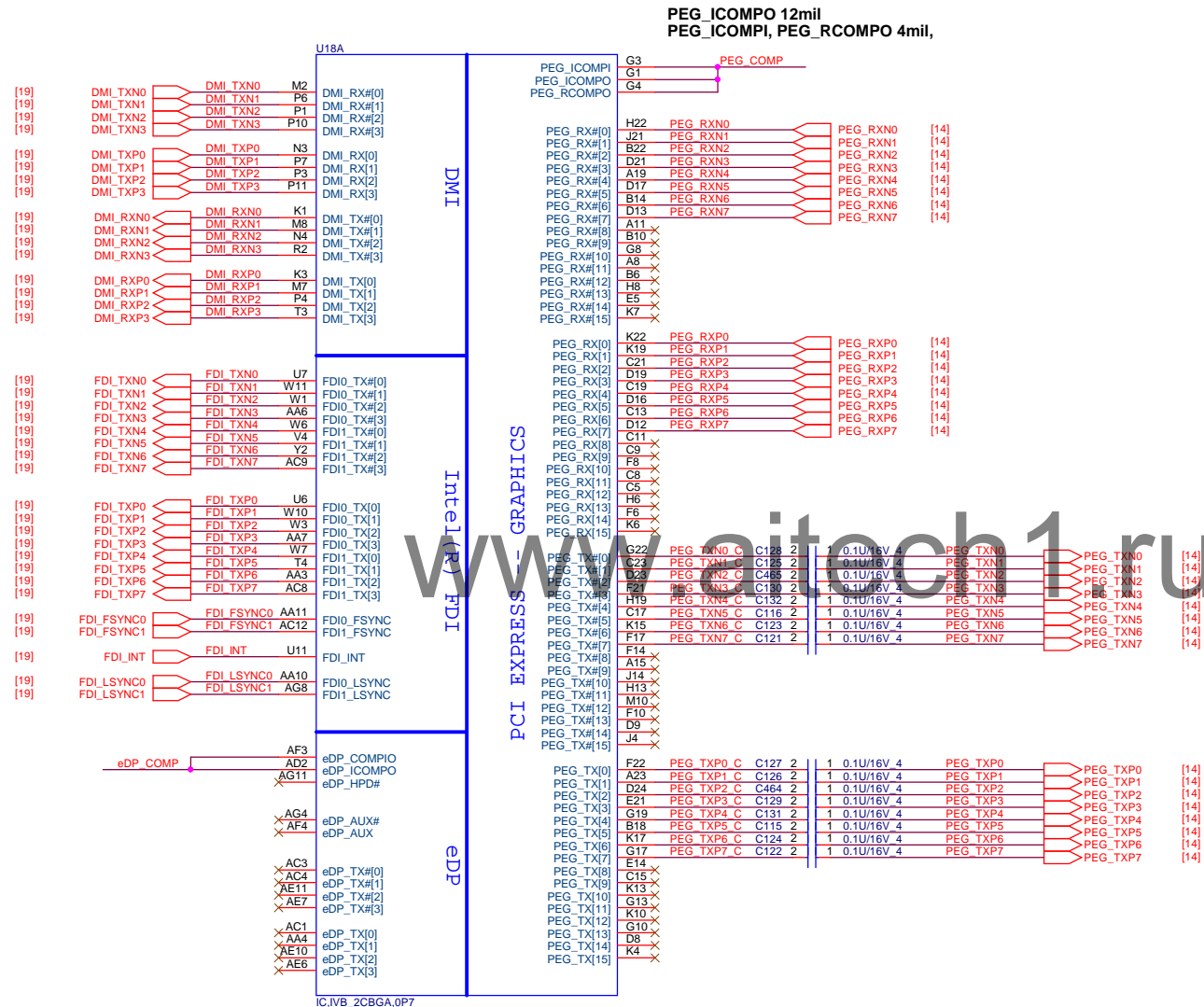
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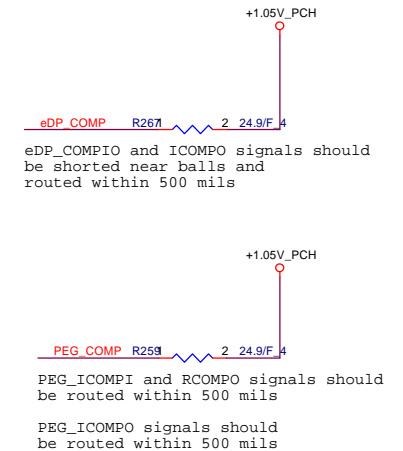
Battery Mode



Ivy Bridge Processor (RESERVED, CFG)



DP & PEG Compensation

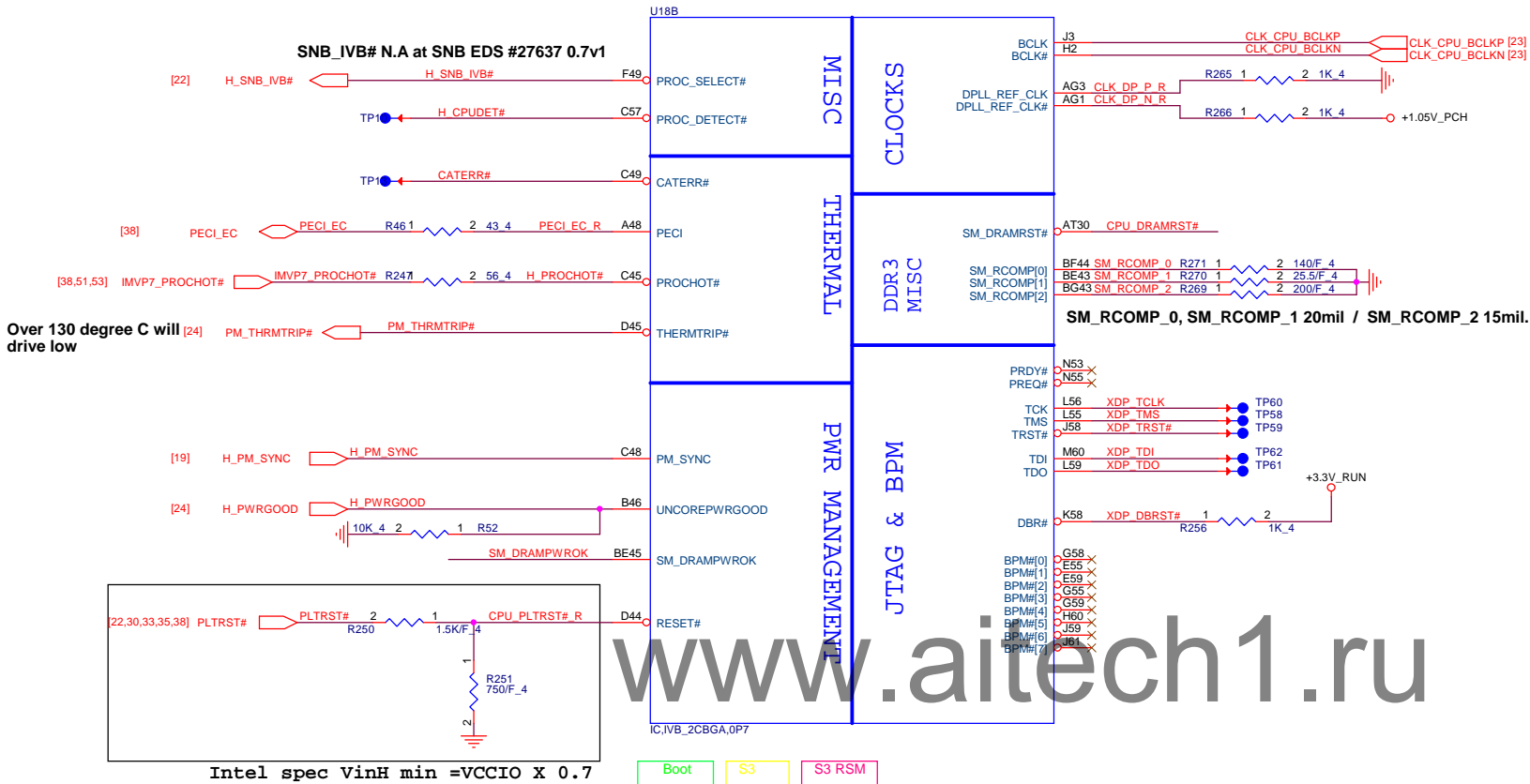


CPU QPN
i7-3540M AJ0QD5J8T00 Quanta B 35W
i5-3230M AJSR0WXQT01 WIN BS 35W
i3-3120M AJSR0TYRT01 WIN BS 35W

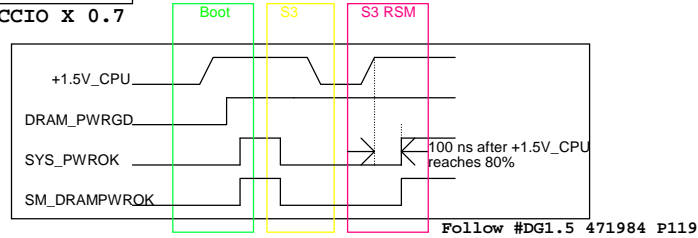


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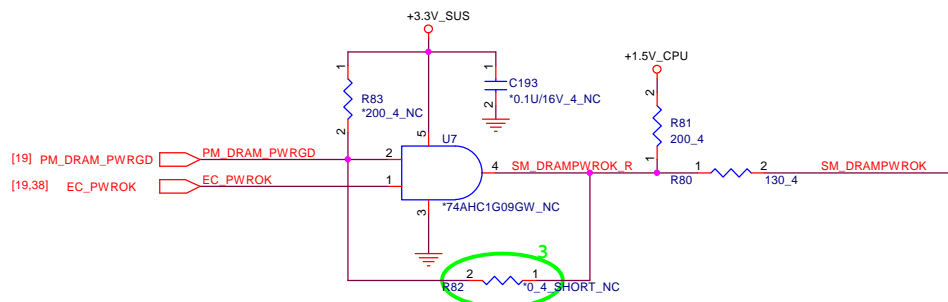
Ivy Bridge Processor (CLK,MISC,JTAG)



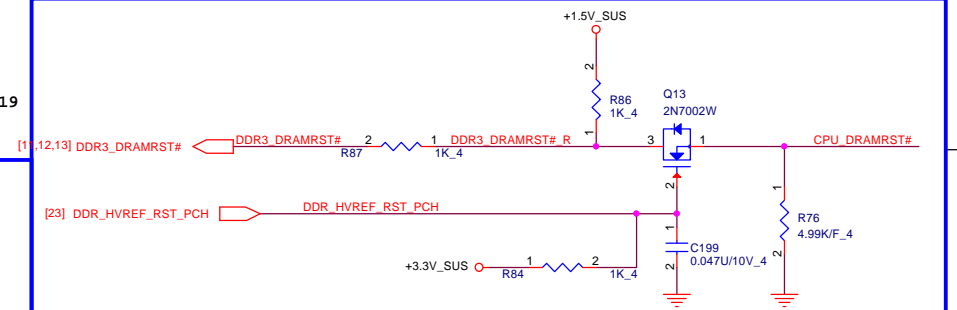
Intel spec VinH min =VCCIO X 0.7



Follow #DG1.5 471984 P128
DDR Power Gating Topology



Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration

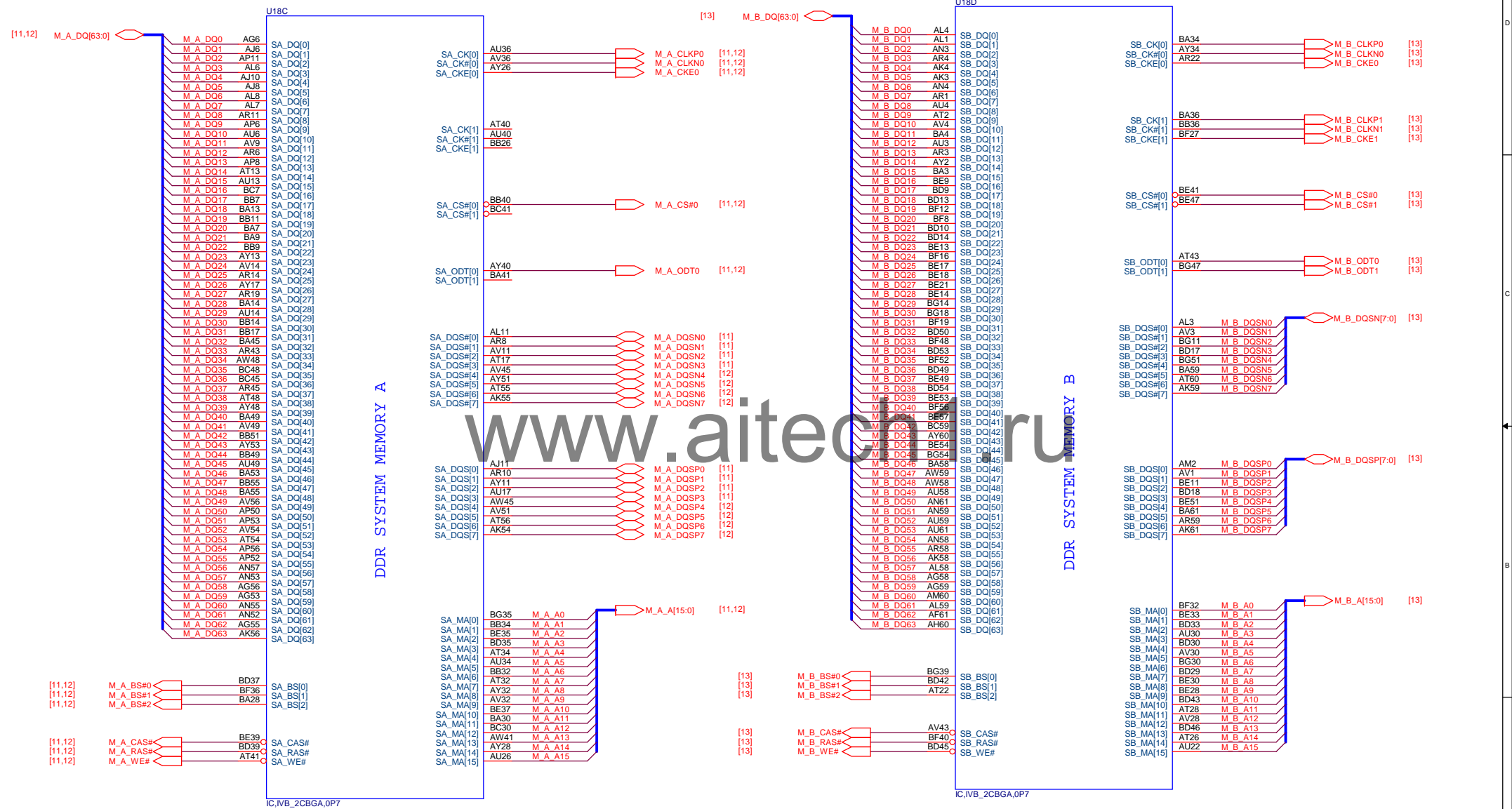


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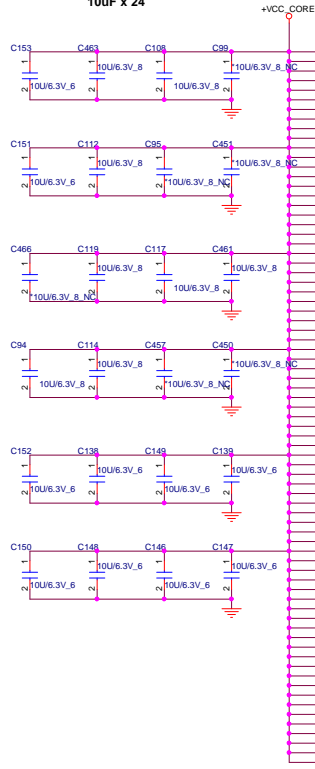
Ivy Bridge 2/5

Ivy Bridge Processor (DDR3)



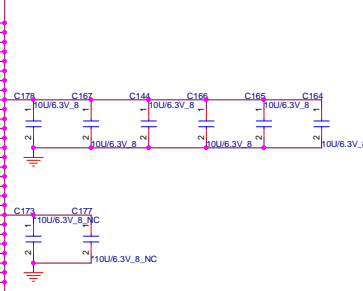
Ivy Bridge Processor

CPU Core Power
SNB: 53A
IVY: 53A
10uF x 24



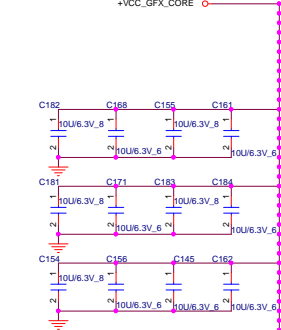
POWER

1.05V_PCH
SNB: 8.5A
IVY: 8.5A
10F x12



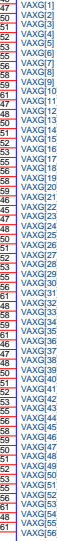
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

CPU VGT
SNB: 21.5A
IVY: 33A
10uF x 12



Ivy Bridge Processor (GRAPHIC POWER)

POWER

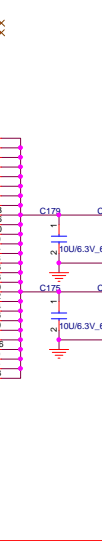


GRAPHICS

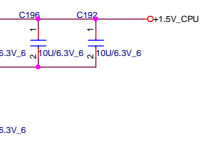
DDR3 - 1.5V RAILS



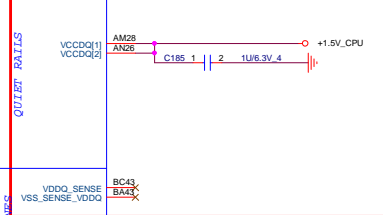
SA RAIL



CPU MCH
SNB: 5A
IVY: 5A
10uF x 6



Only BGA

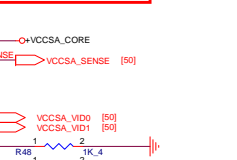
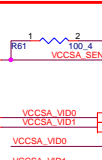


SENSE LINES

1.8V RAIL

SA RAIL

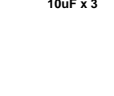
VCCSA VID Lines



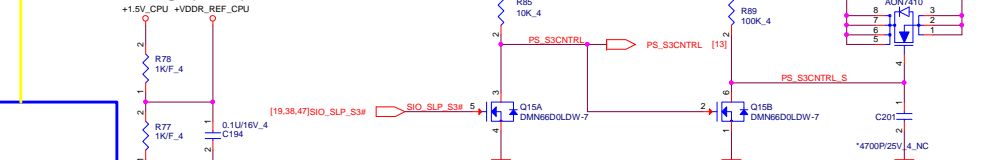
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CPU VCCPL
SNB: 1.2A
IVY: 1.2A
10uF x 1

CPU SA
SNB: 6A
IVY: 6A
10uF x 3



Take care Q3 Vgs(MAX)=2.5



Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

VR_SVID_CLK

Place PU resistor close to CPU

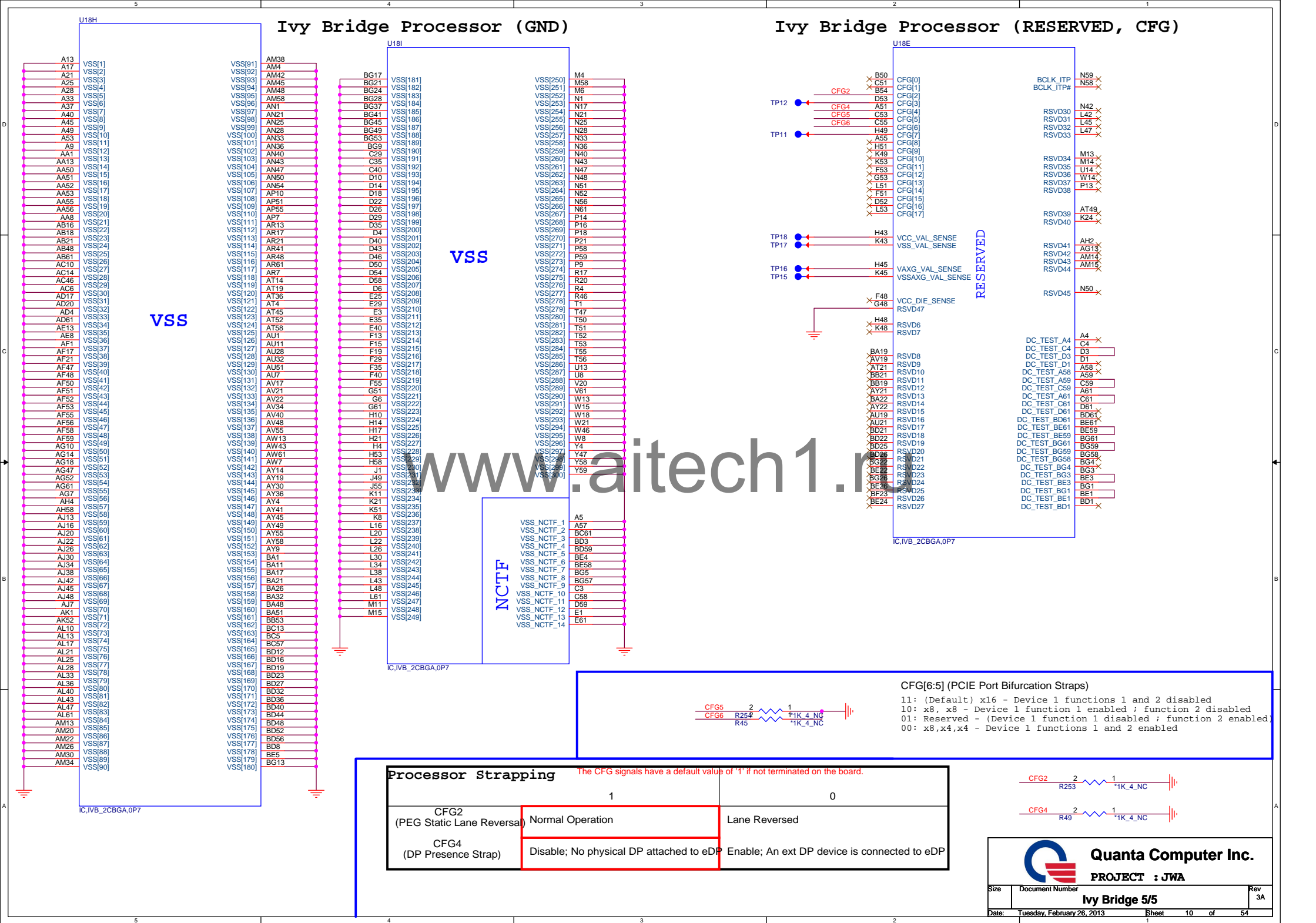
SVID DATA

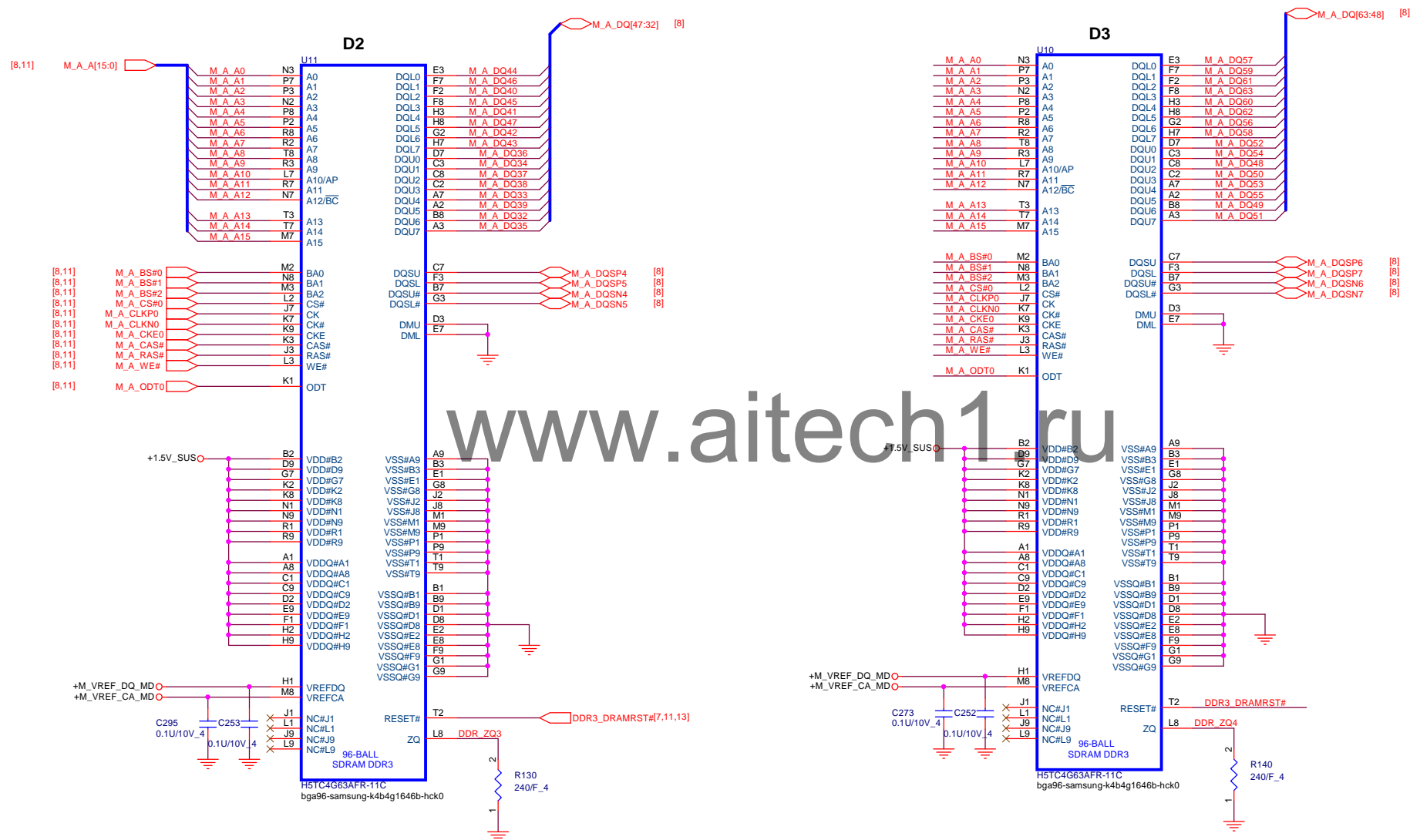
VR_SVID_DATA

Place PU resistor close to CPU

SVID ALERT

VR_SVID_ALERT

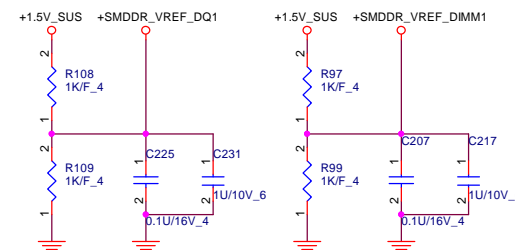
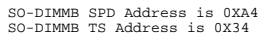


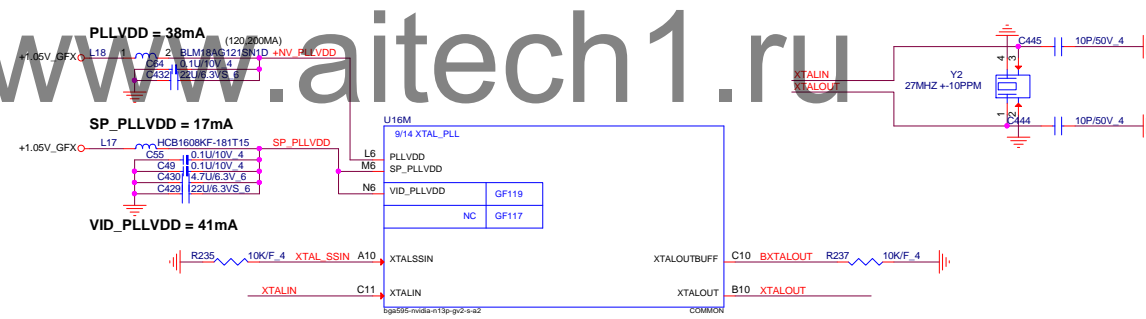
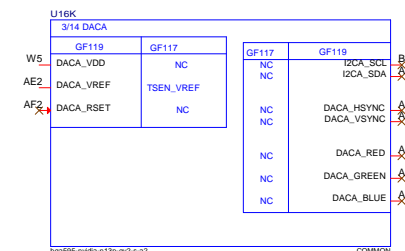
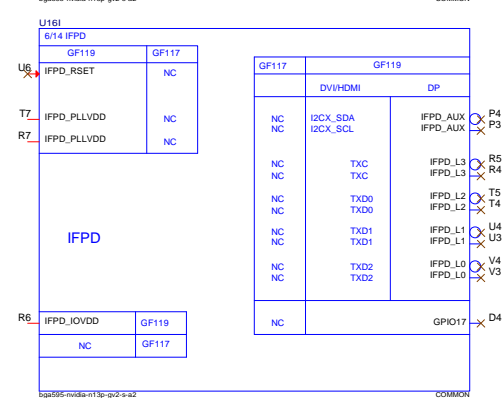


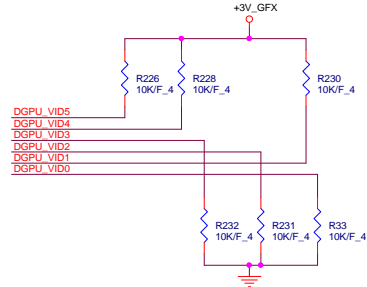
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PROJECT : JWA

Size	Document Number	Rev
		3A
DDR3 (A) On Board B,1Rank		
Date:	Tuesday, February 26, 2013	Sheet 12 of 54

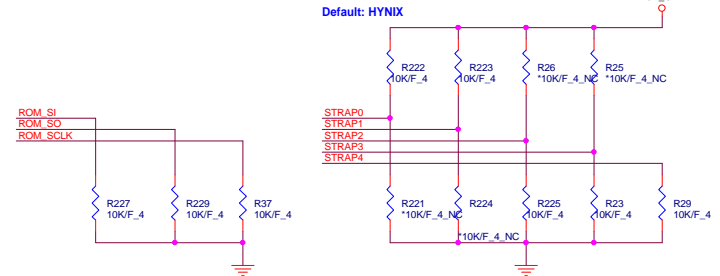
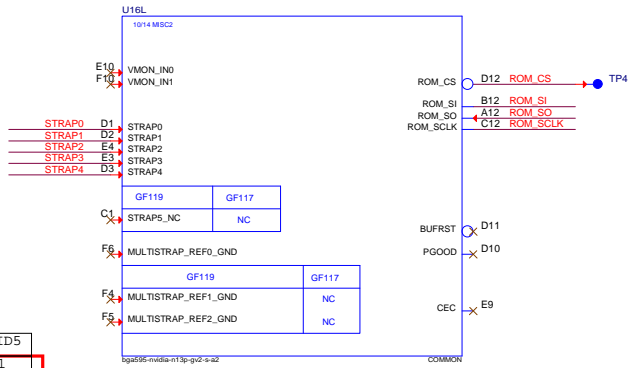






**N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010**

	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GV2	0.875V	0	1	0	0	1	1



Binary Strap Mode Mapping

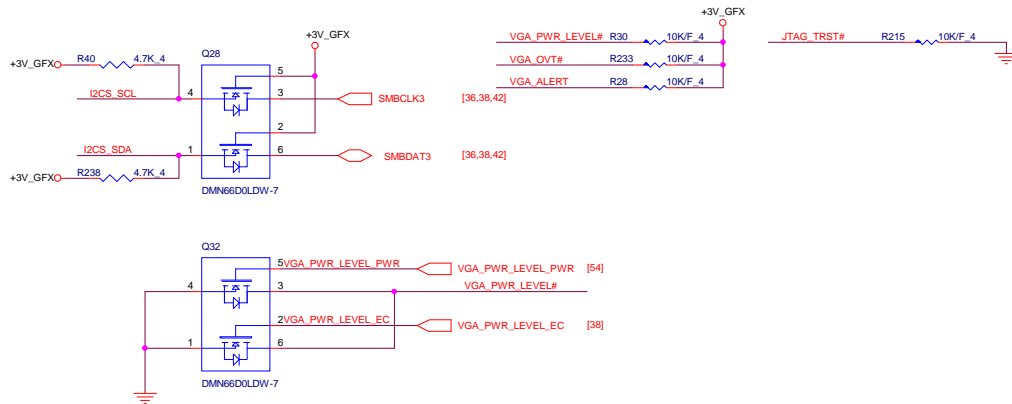
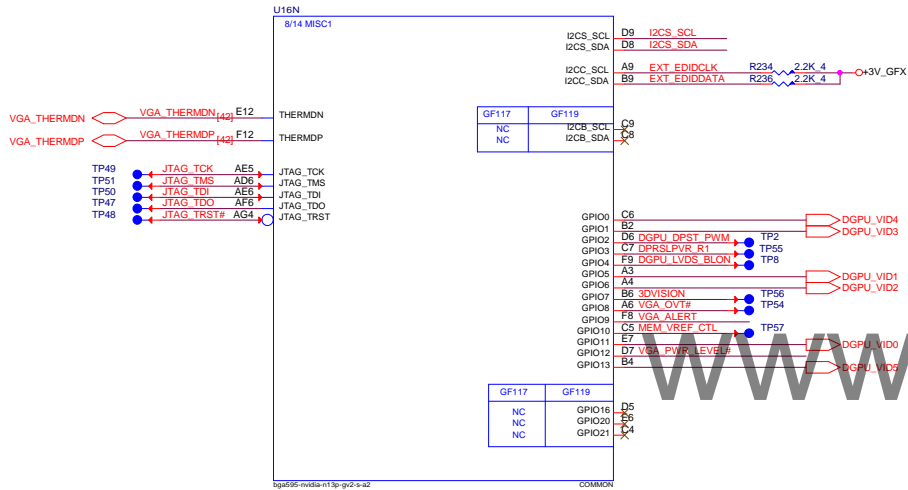
Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG[1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

**ROM_SI
VRAM Configuration Table**

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
0000	Reserved	Reserved		
1100	IC SDRAM(96P)H5TQ2G63DFR-11C(FBGA)	HYNIX	H5TQ2G63DFR-11C	AKD5MGWTW16
2Gb 1011	IC SDRAM(96P)K4W2G1646E-BC11(FBGA)	SAMSUNG	K4W2G1646E-BC11	AKD5MGWT520
4Gb 0011	IC SDRAM(96P)H5TQ4G63MFR-11C(FBGA)	HYNIX	H5TQ4G63MFR-11C	AKD5PGTW04
4Gb 0001	IC SDRAM(96P)K4W4G1646B-HC11(FBGA)	SAMSUNG	K4W4G1646B-HC11	AKD5MGWT516
4Gb 0101	IC SDRAM(96P)MT41K256M16HA-107G-E(FBGA)	Micron	MT41K256M16HA-107G	AKD5PGSTL00

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

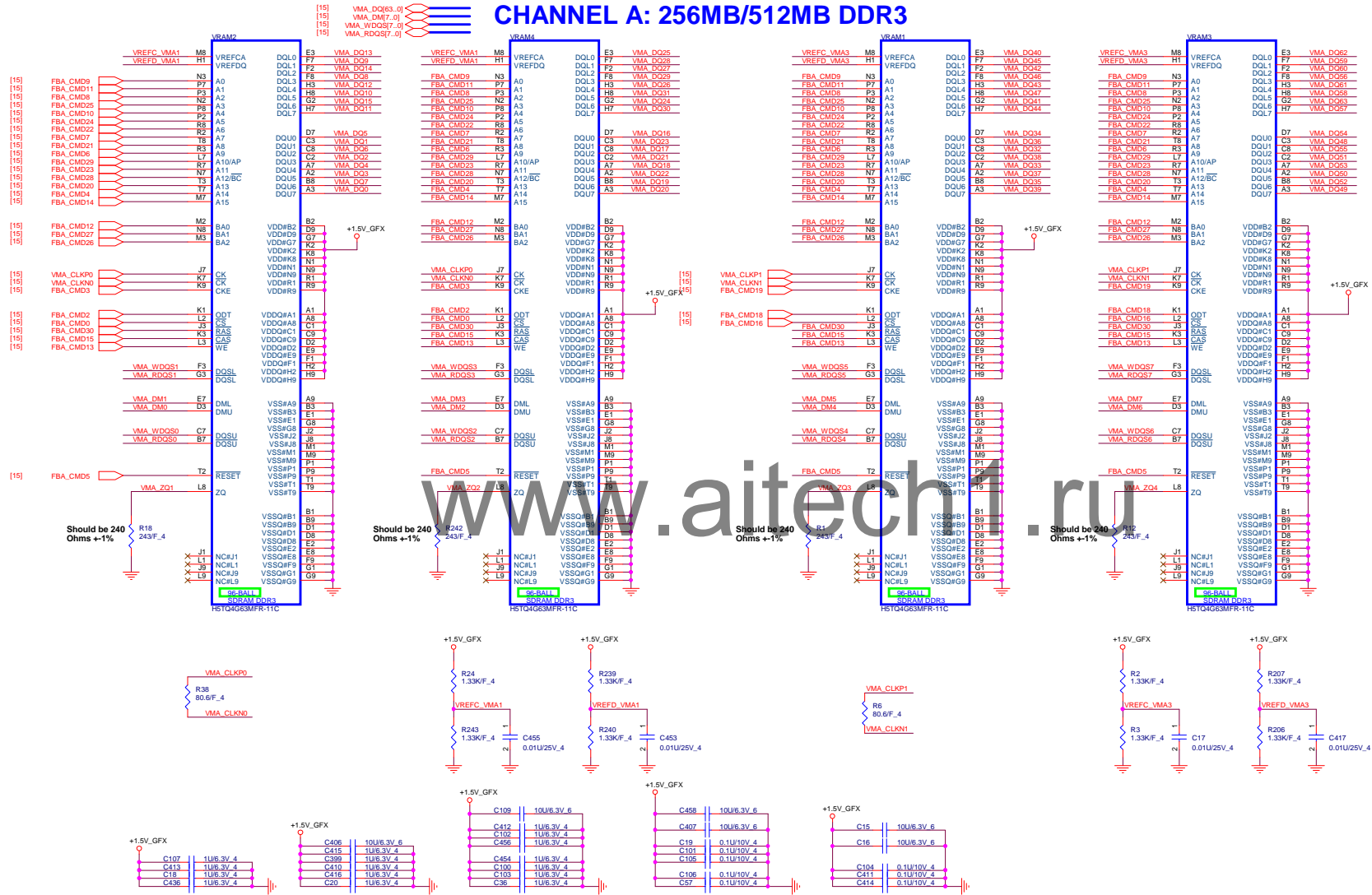


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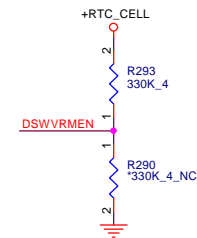
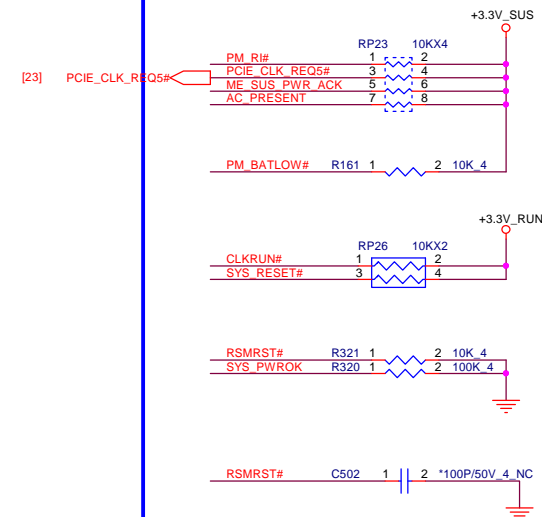
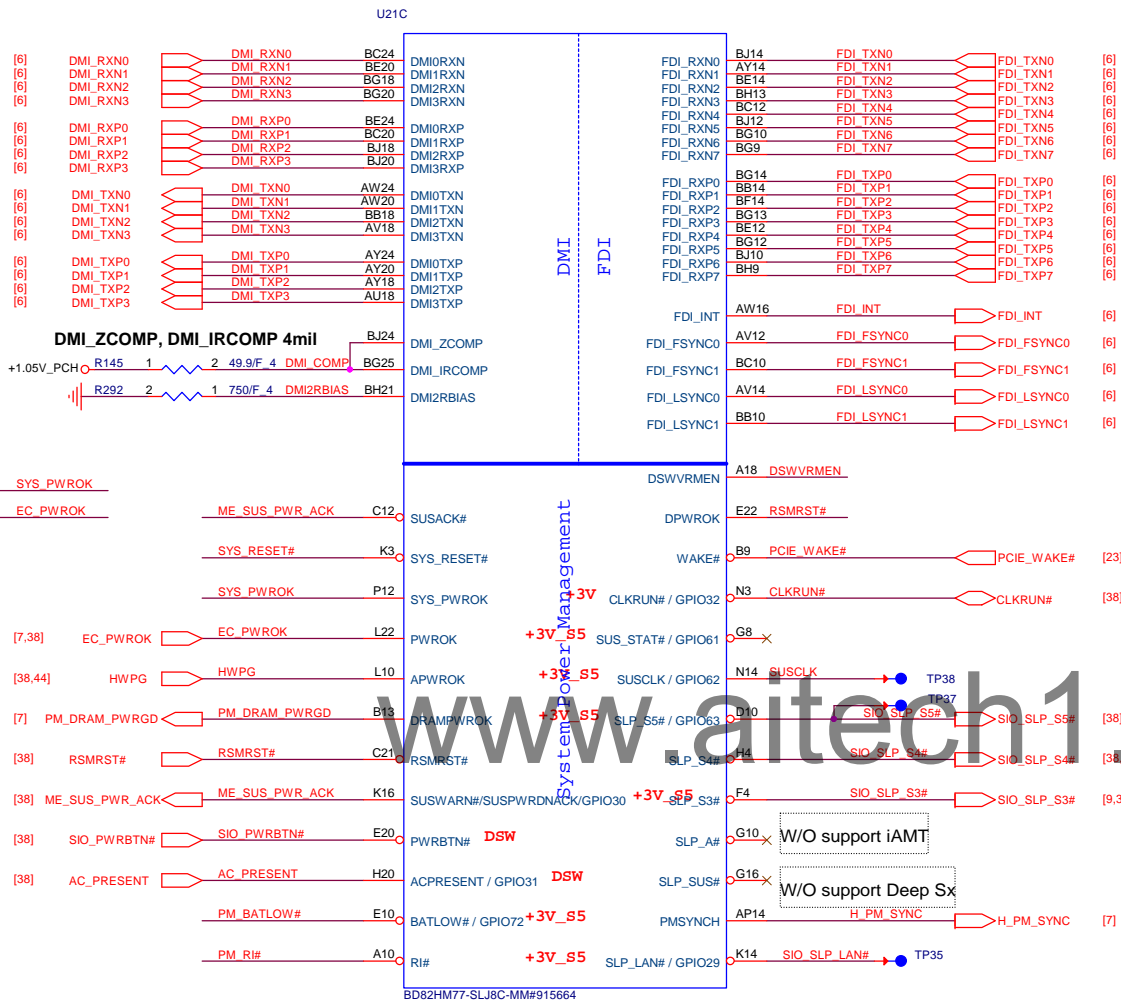
900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT516
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5PGWTW04

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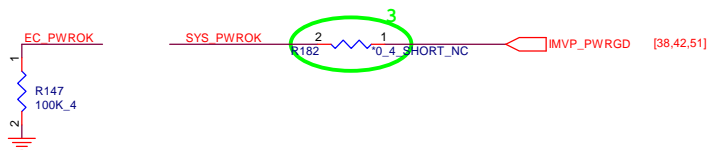
CHANNEL A: 256MB/512MB DDR3



Cougar Point/Panther Point (DMI,FDI,PM)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

**Quanta Computer Inc.**

PROJECT : JWA

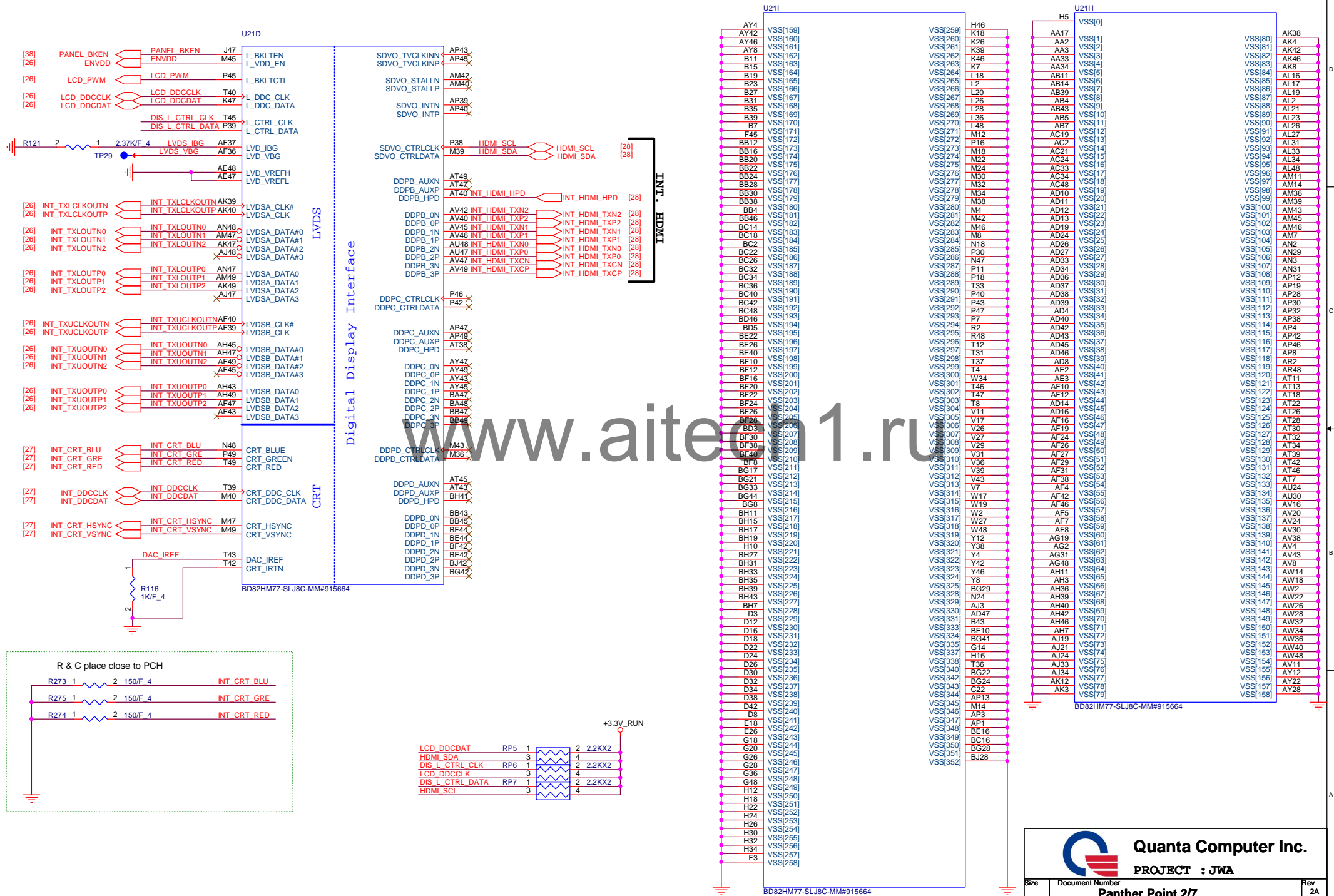
Size	Document Number
	Panther Point 1/7

Date: Tuesday, February 26, 2013 Sheet 19 of 54

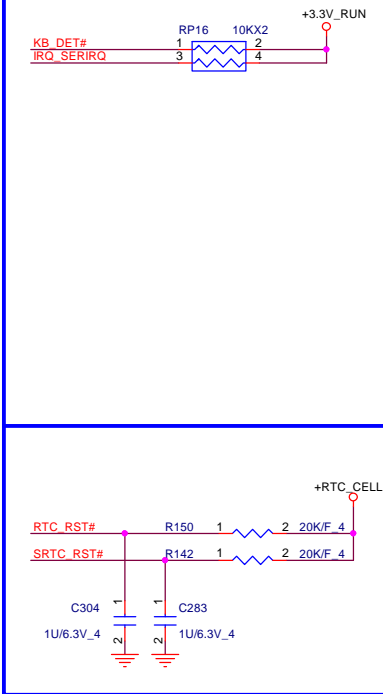
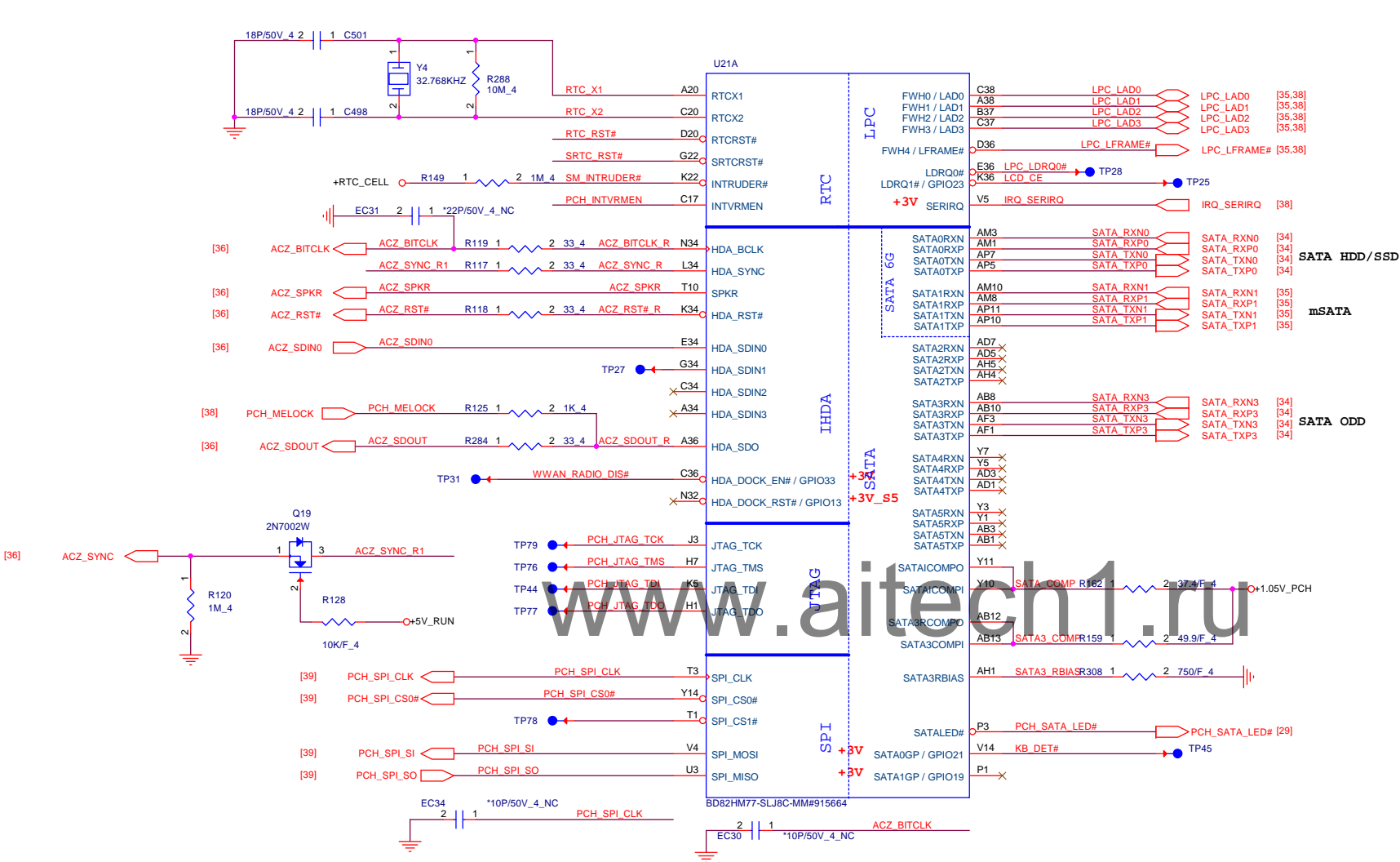
Re	
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Cougar Point/Panther Point (LVDS,DDI)

Cougar Point/Panther Point (GND)



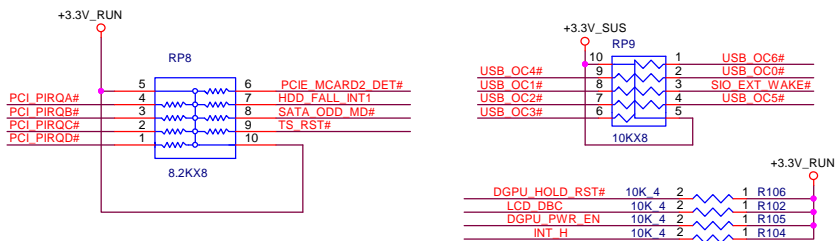
Cougar Point/Panther Point (HDA,JTAG,SATA)



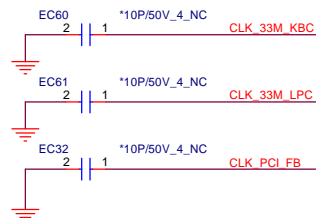
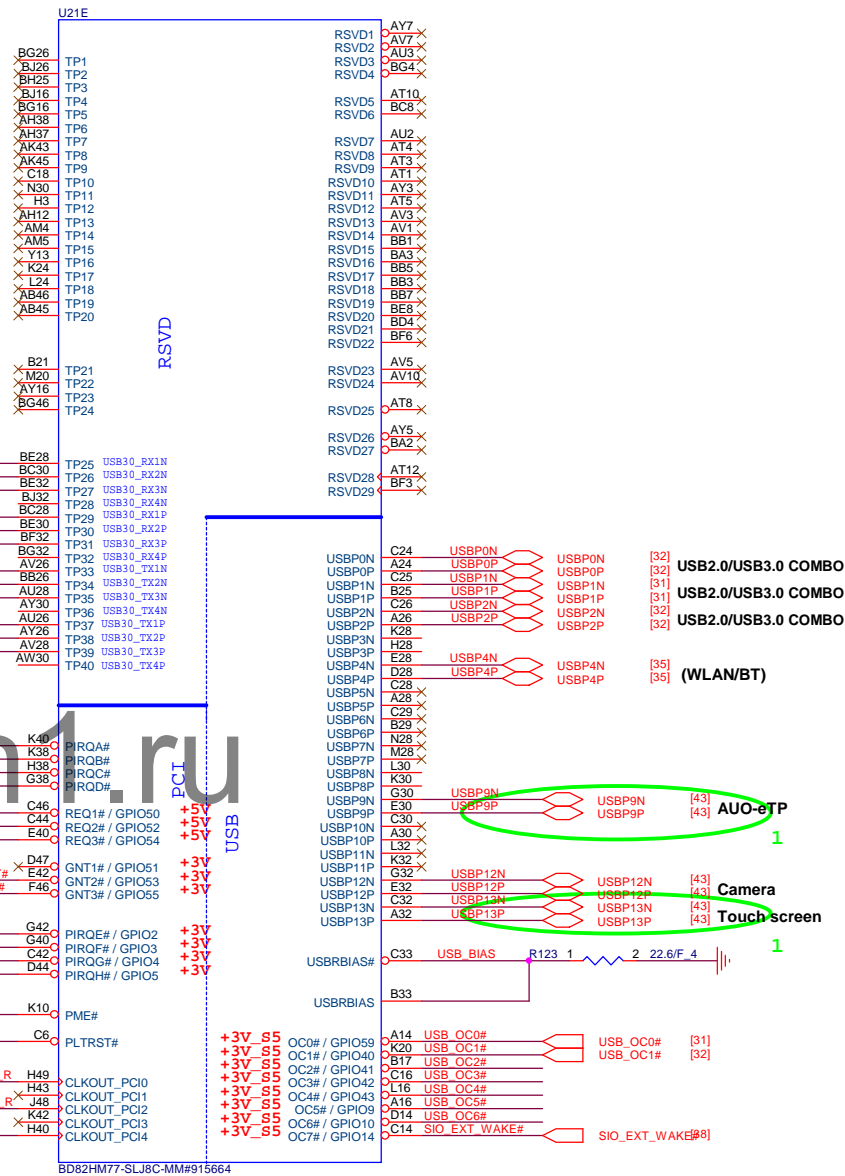
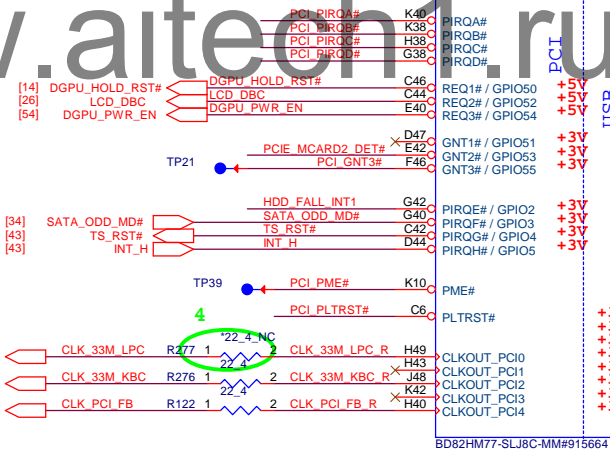
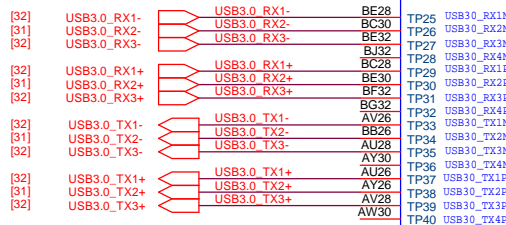
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○R294 1 2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○R115 1 2 1K 4 ACZ_SYNC_R

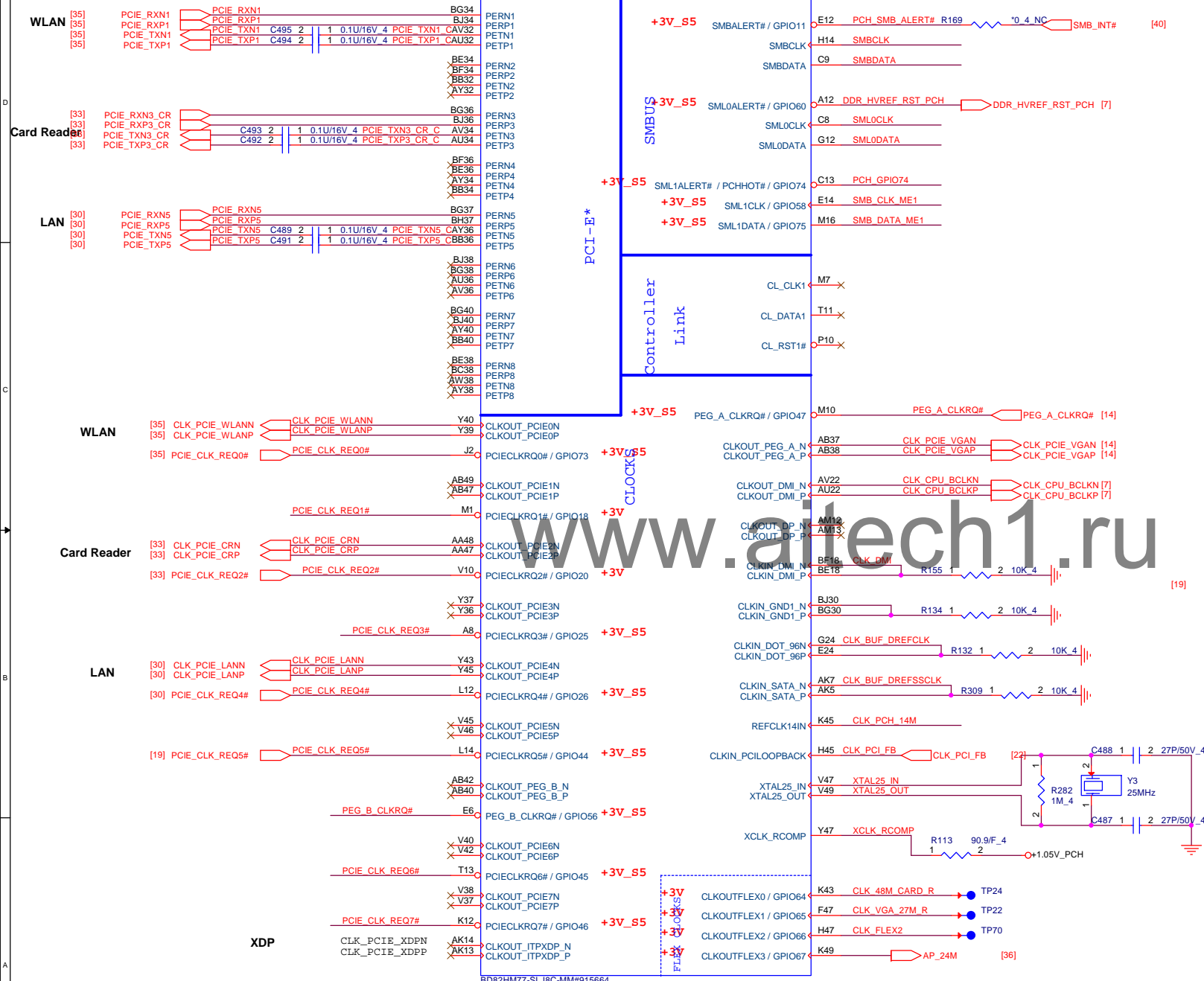
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



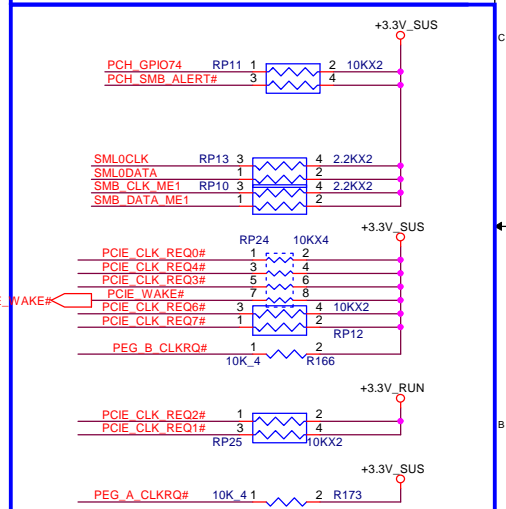
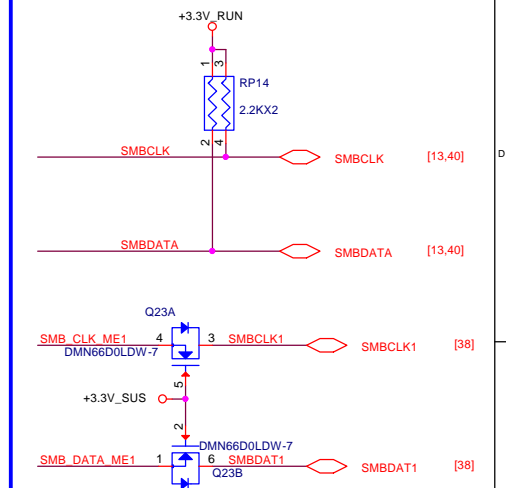
Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESl strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]												
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
<p>R178 2 1 2.2K 4 +1.8V_RUN 2 1 DF_TV5 DF_TV5 [24] R177 2 1 1K 4 H_SNB_IVB# H_SNB_IVB# [7]</p>												



Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

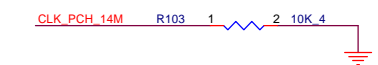


SMBus/Pull-up(CLG)



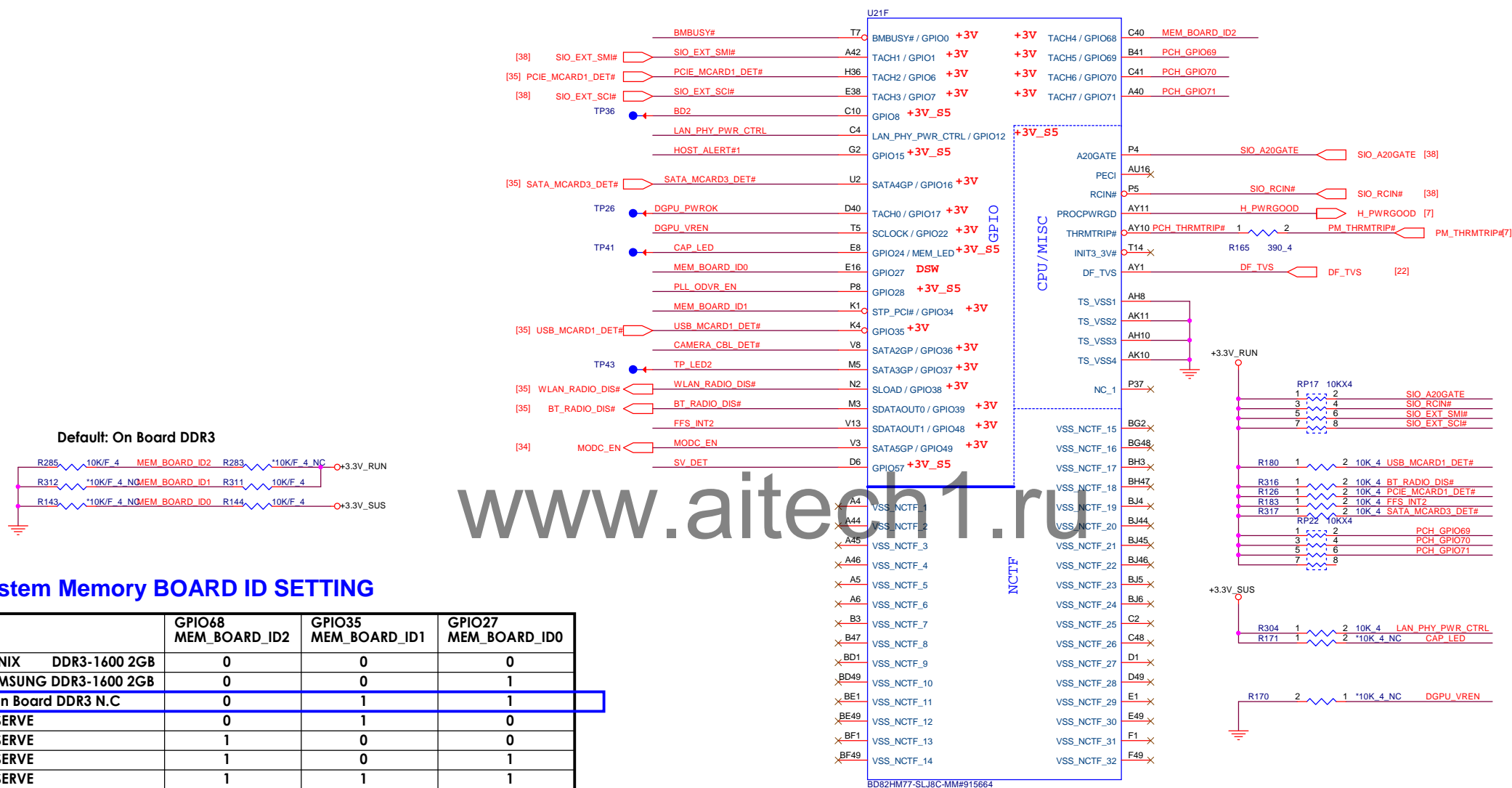
CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode



CLKOUTFLEX0 / GPIO64	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX1 / GPIO65	• 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX2 / GPIO66	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX3 / GPIO67	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
	• 27/14.318 output to SIO/48/24 MHz (Default)

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

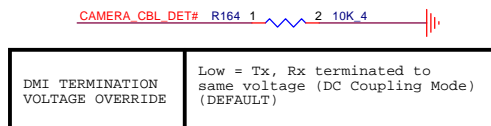


System Memory BOARD ID SETTING

	GPIO68 MEM_BOARD_ID2	GPIO35 MEM_BOARD_ID1	GPIO27 MEM_BOARD_ID0
HYNIX DDR3-1600 2GB	0	0	0
SAMSUNG DDR3-1600 2GB	0	0	1
On Board DDR3 N.C	0	1	1
RESERVE	0	1	0
RESERVE	1	0	0
RESERVE	1	0	1
RESERVE	1	1	1
RESERVE	1	1	0

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

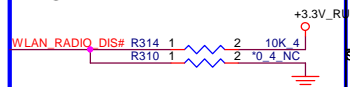
R168 1 2 *1K_4_NC PLL_ODVR_EN



BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up
(8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and
100 ohm on this net for validation purpose.

MFG-TEST



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

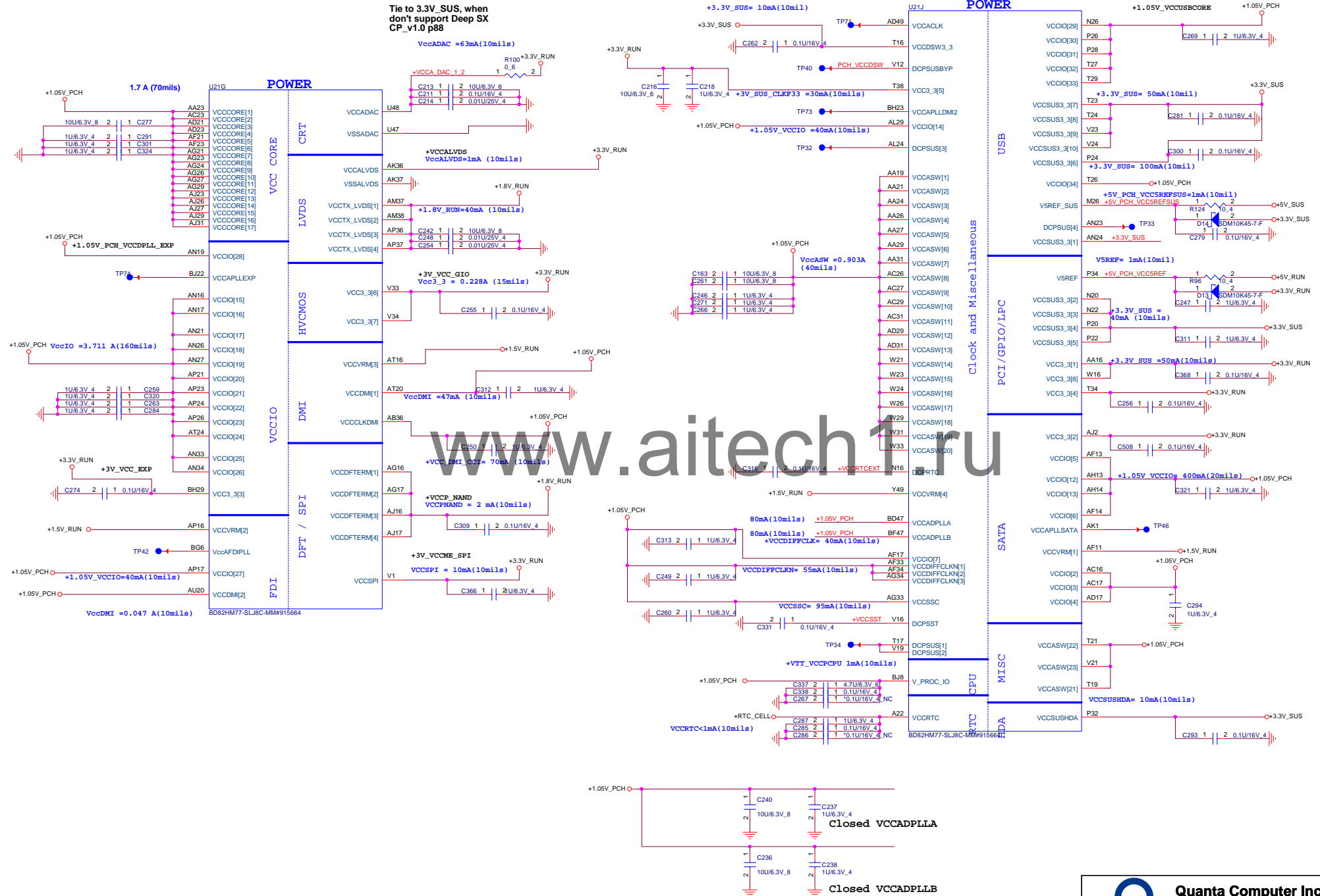


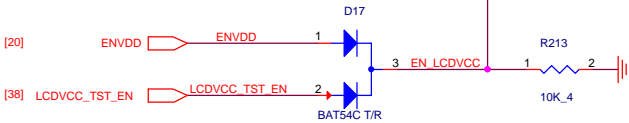
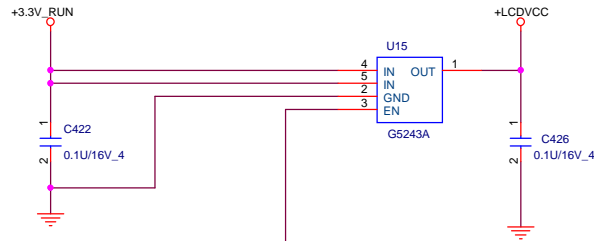
Quanta Computer Inc.
PROJECT : JWA

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	Panther Point 6/7	3A
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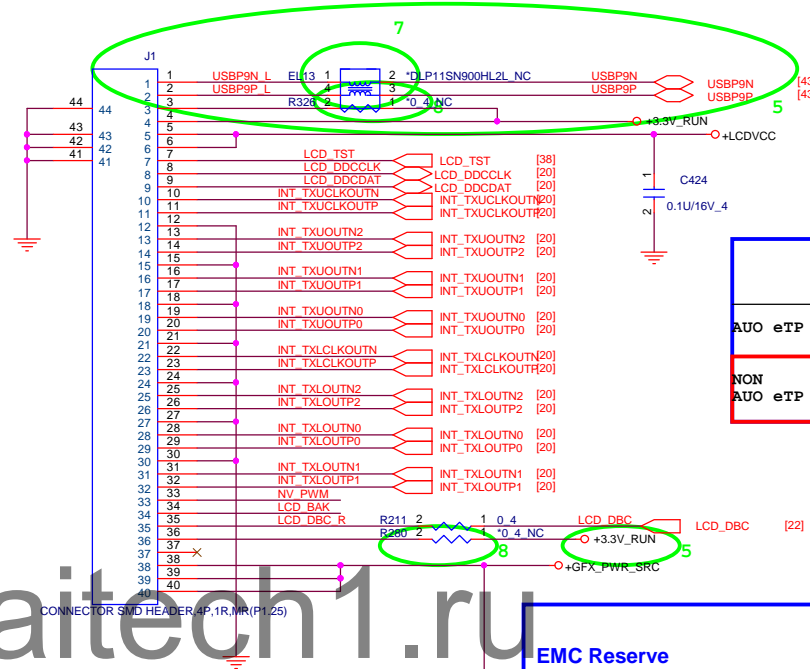
Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)





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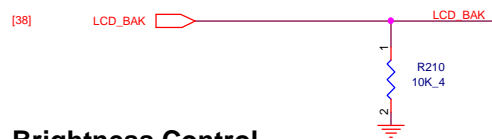
	EL13	R326	R280
AUO eTP	O	O	O
NON AUO eTP	X	X	X

EMC Reserve

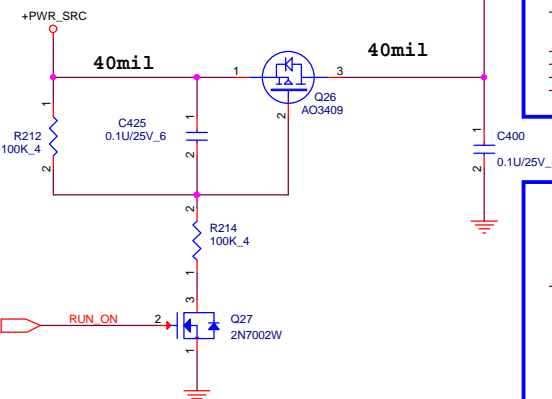
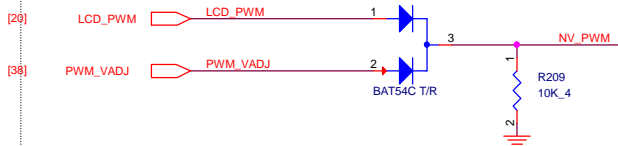
INT TXCLKOUTN	EC46	1	2	3.3P	INT TXCLKOUTP
INT TXOUTN2	EC42	1	2	3.3P	INT TXOUTP2
INT TXOUTN1	EC43	1	2	3.3P	INT TXOUTP1
INT TXOUTN0	EC47	1	2	3.3P	INT TXOUTP0

INT TXCLKOUTN	EC44	1	2	3.3P	INT TXCLKOUTP
INT TXOUTN2	EC40	1	2	3.3P	INT TXOUTP2
INT TXOUTN1	EC45	1	2	3.3P	INT TXOUTP1
INT TXOUTN0	EC41	1	2	3.3P	INT TXOUTP0

Backlight Enable

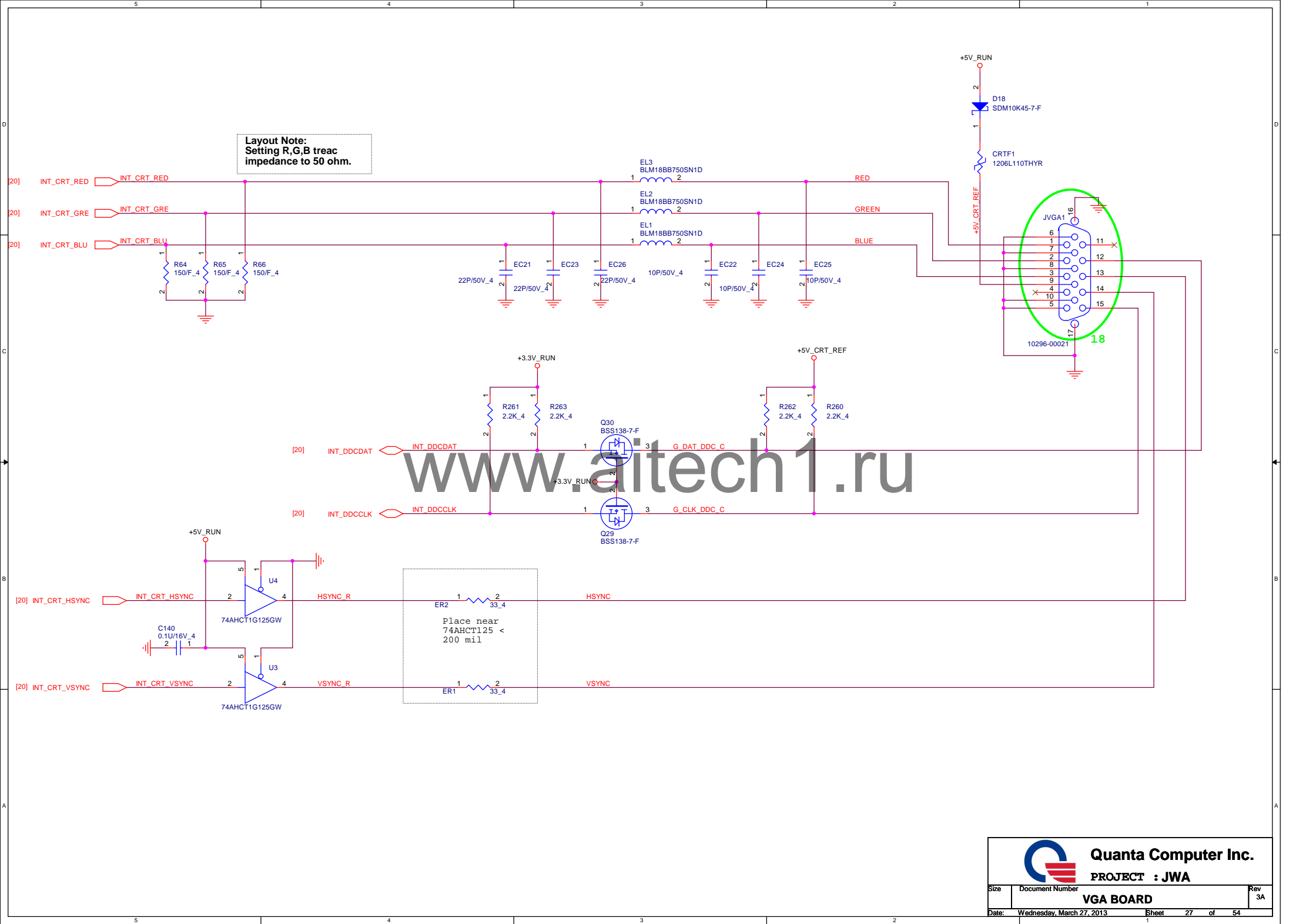


Brightness Control



Close to J1

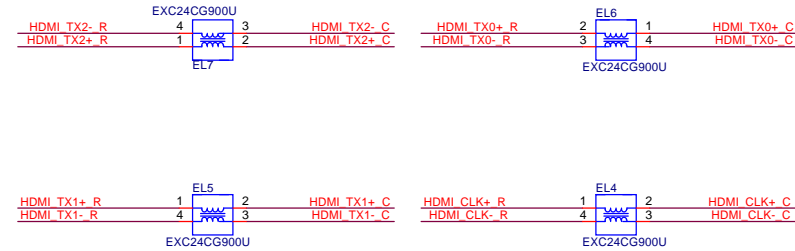




HDMI

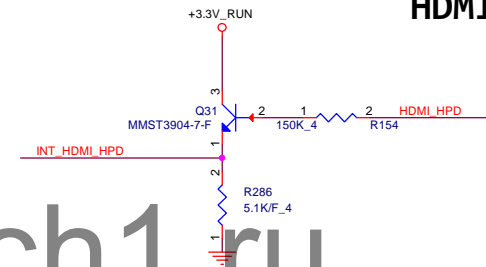
[20] INT_HDMI_TXP2	INT_HDMI_TXP2	C371	1	2	0.1U/16V_4	HDMI TX2+ R
[20] INT_HDMI_TXN2	INT_HDMI_TXN2	C369	1	2	0.1U/16V_4	HDMI TX2- R
[20] INT_HDMI_TXP1	INT_HDMI_TXP1	C348	1	2	0.1U/16V_4	HDMI TX1+ R
[20] INT_HDMI_TXN1	INT_HDMI_TXN1	C344	1	2	0.1U/16V_4	HDMI TX1- R
[20] INT_HDMI_TXP0	INT_HDMI_TXP0	C353	1	2	0.1U/16V_4	HDMI TX0+ R
[20] INT_HDMI_TXN0	INT_HDMI_TXN0	C362	1	2	0.1U/16V_4	HDMI TX0- R
[20] INT_HDMI_TXCP	INT_HDMI_TXCP	C339	1	2	0.1U/16V_4	HDMI CLK+ R
[20] INT_HDMI_TXCN	INT_HDMI_TXCN	C335	1	2	0.1U/16V_4	HDMI CLK- R
[20] HDMI_SCL	HDMI_SCL					
[20] HDMI_SDA	HDMI_SDA					
[20] INT_HDMI_HPD	INT_HDMI_HPD					

Reserve for EMI and close to HDMI CONN



HDMI_HPD spec VinH_min=2.0V

HDMI HPD

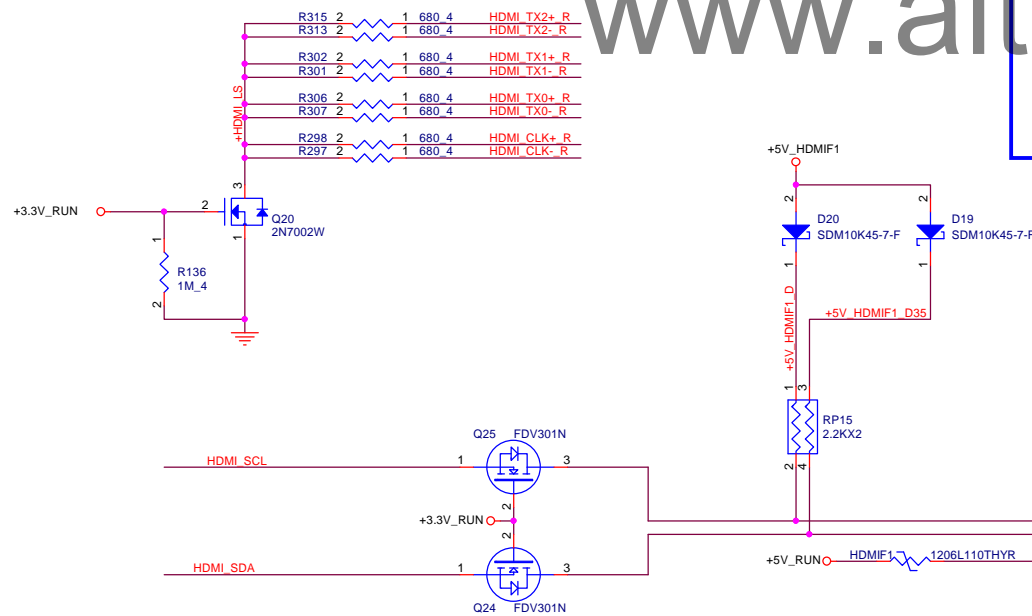


$$I_B = (5V - 0.7V) / (150K + (70 + 1) 5.1K) = 8.4\mu A$$

$$I_E = (1 + 70) \times 8.4\mu A = 596.4\mu A$$

$$V_E = 596.4\mu A \times 5.1K = 3.04V$$

$$B = 70$$



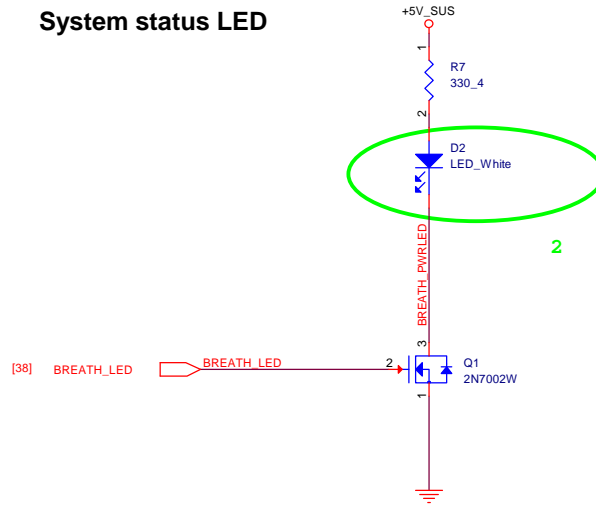
HDMI Conn.



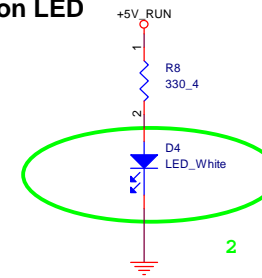
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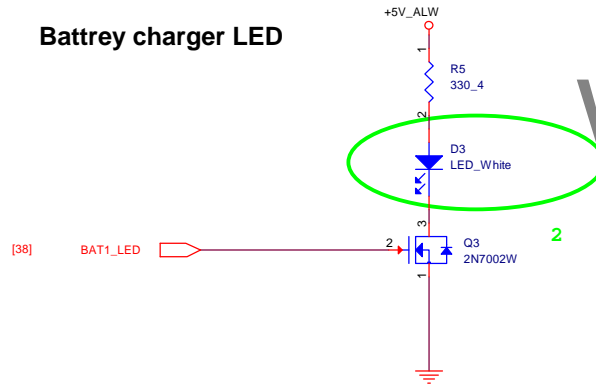
System status LED



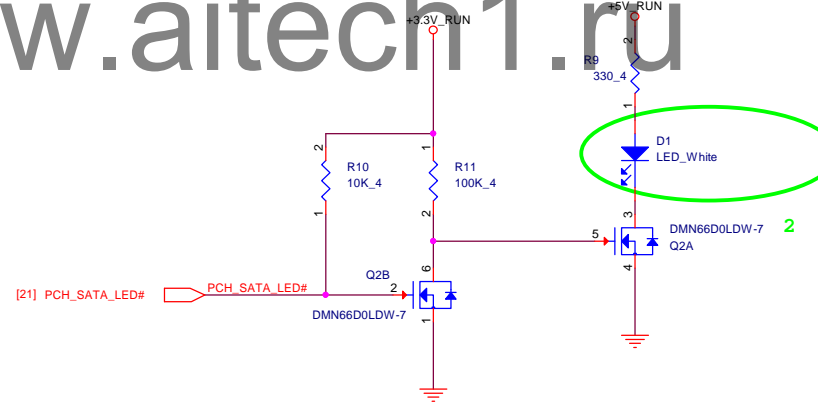
Power Button LED



Battery charger LED



HDD access LED

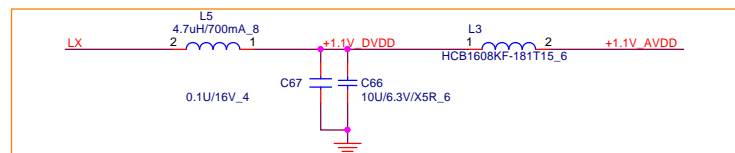
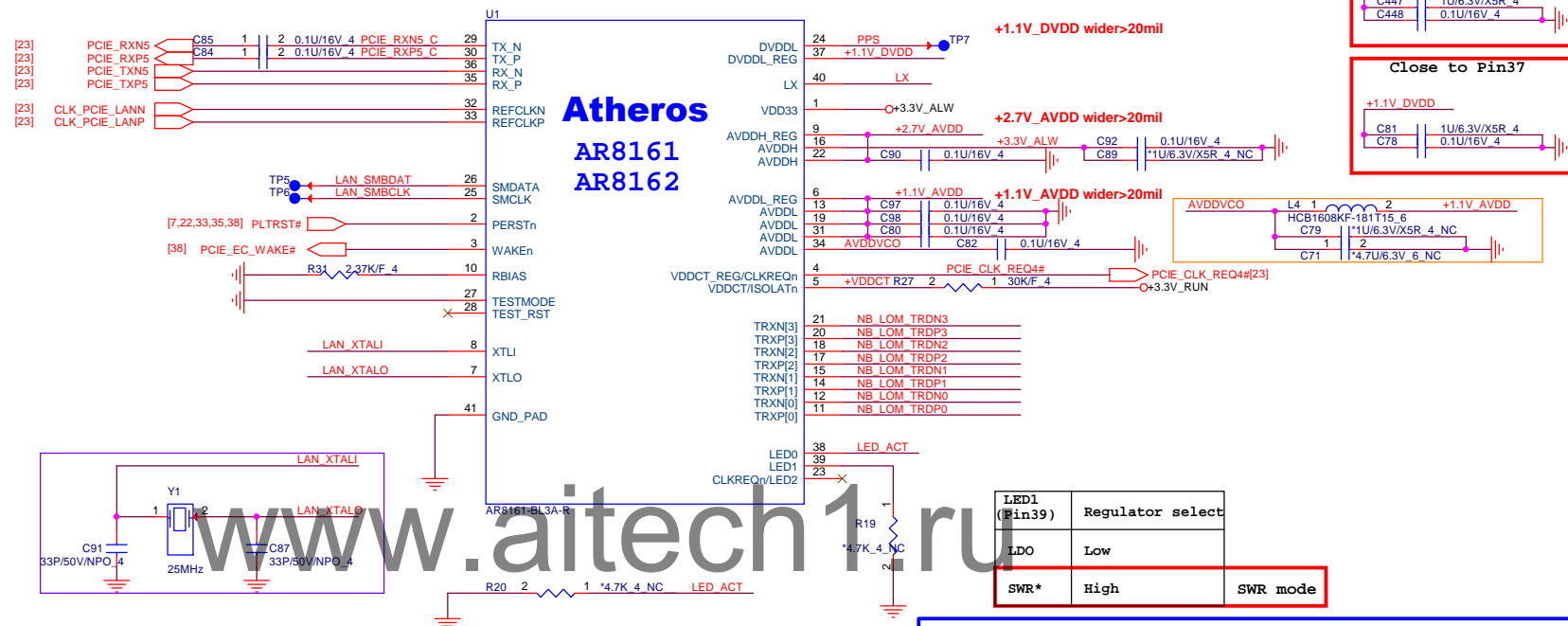
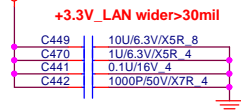


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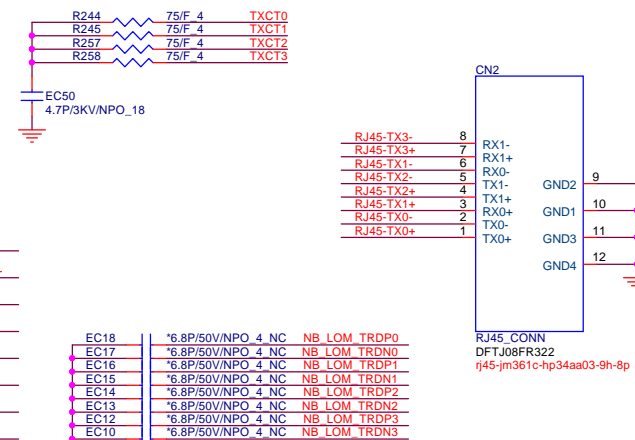
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+3.3V_ALW

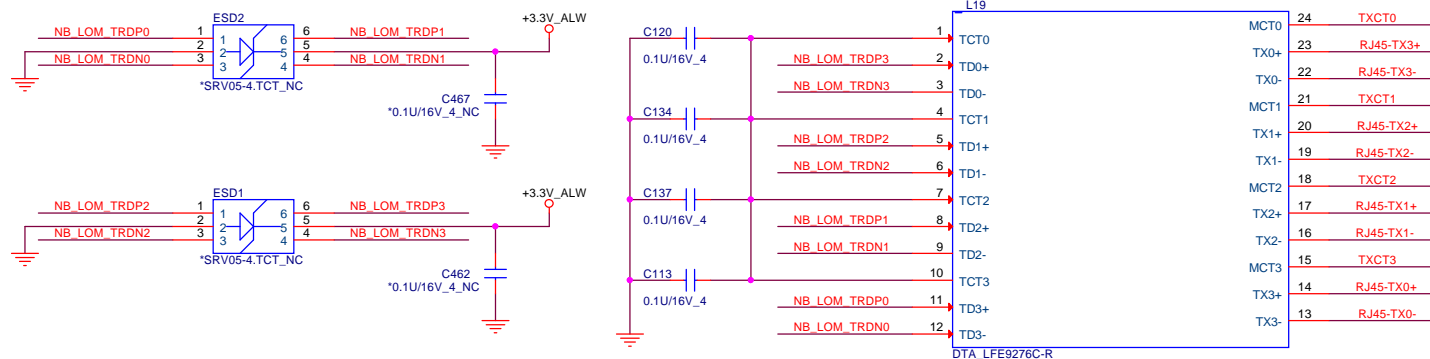


	Core voltage select	
LED_ACT	High core voltage	Low core voltage
	1	0

RJ-45 Connector



Place ESD diodes as
close as TRANSFORMER

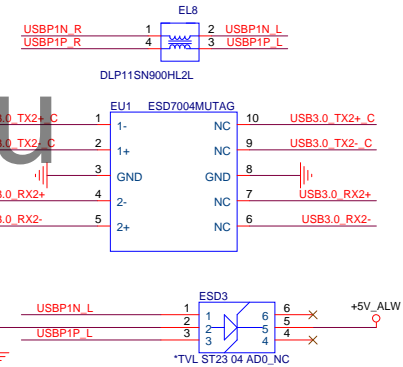
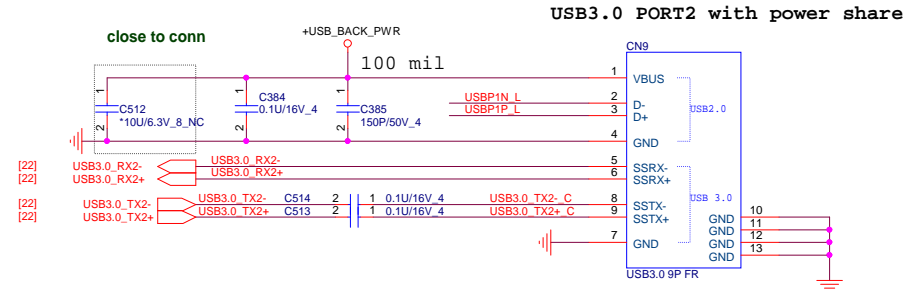
**Quanta Computer Inc.**

PROJECT : JWA

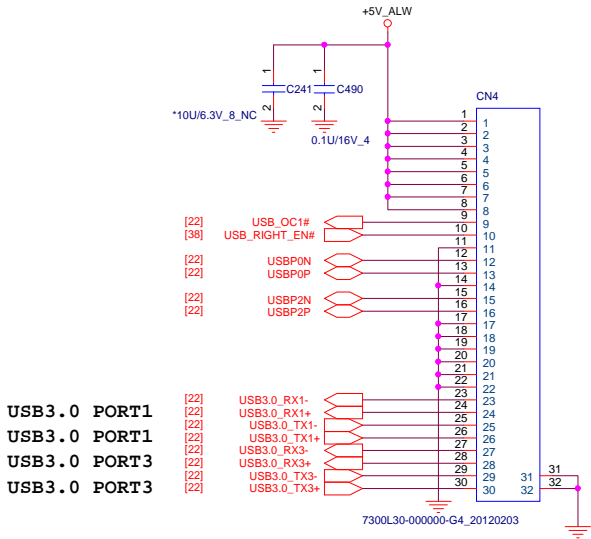
Size	Document Number	Rev
	LAN (AR8161A / AR8162)colay	3A
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USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

	R109	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

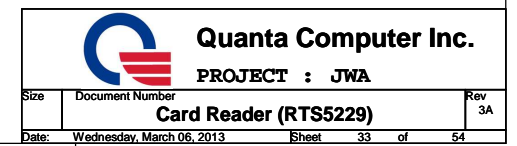


USB CONN*2 (USB3.0 port 0 & 3) BTB CN

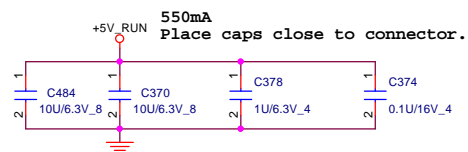
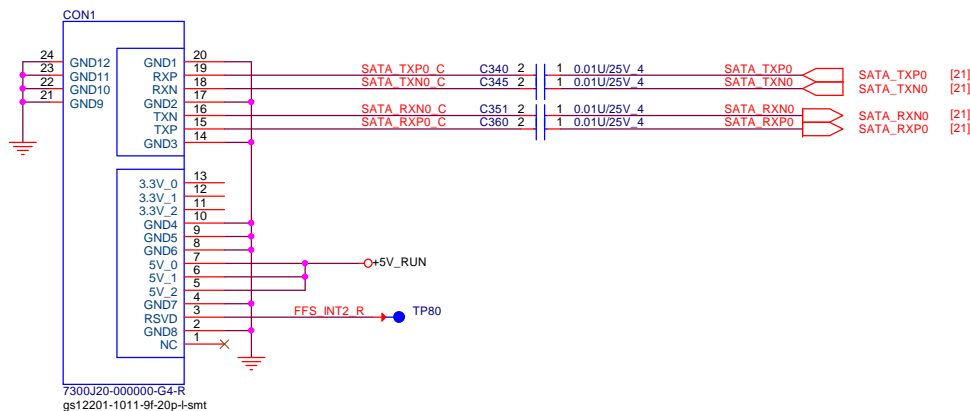


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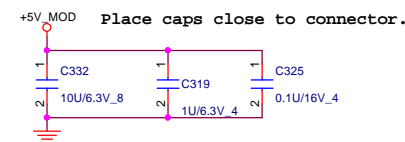
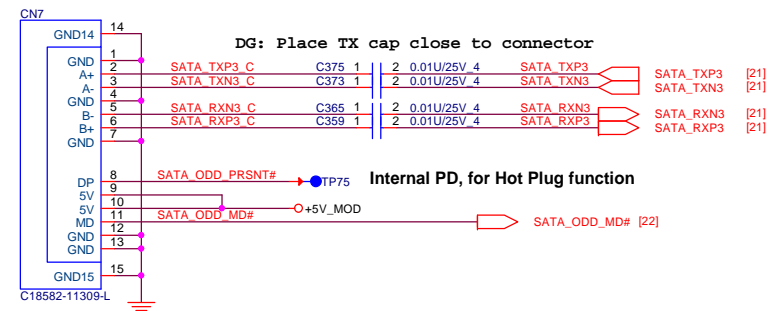
SD / MMC
CARD READER



HDD

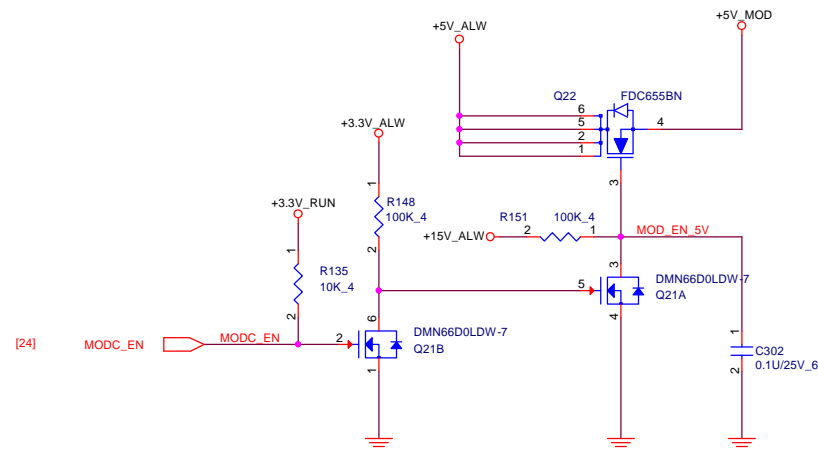


ODD



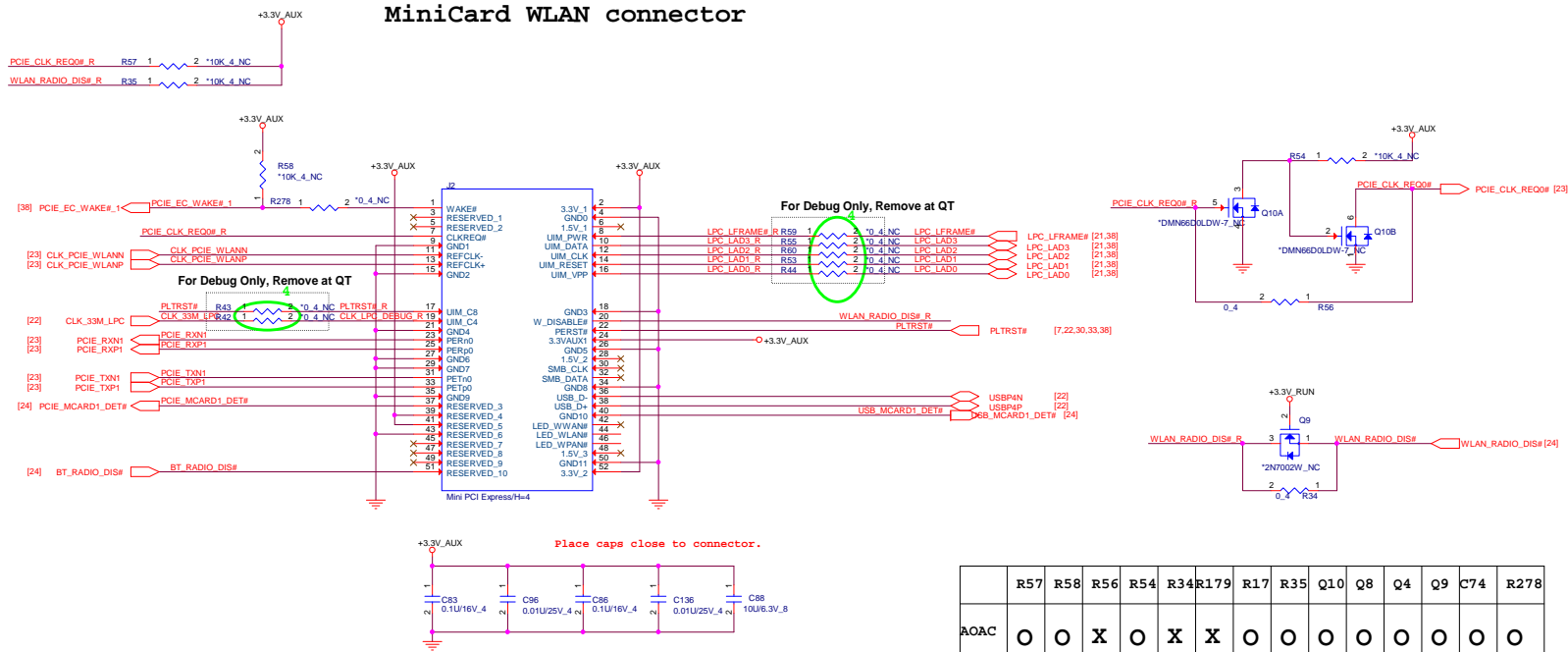
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Support Zero power ODD

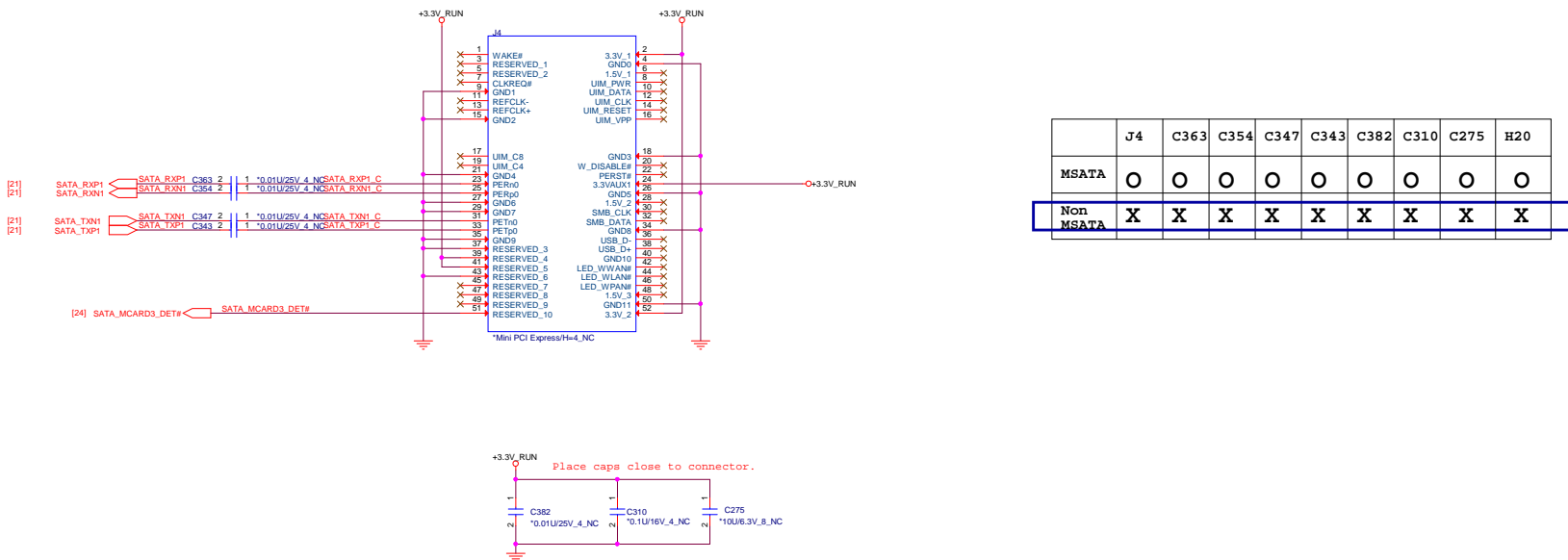


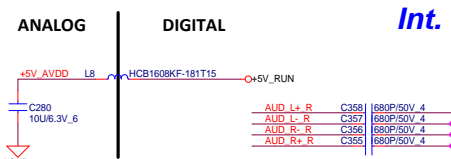
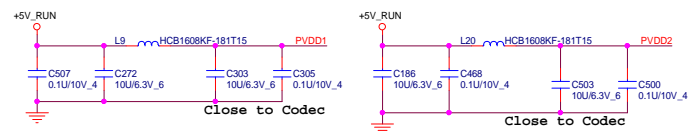
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MiniCard WLAN connector



mSATA Connector



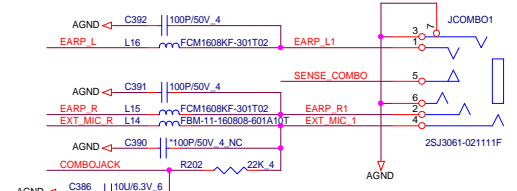
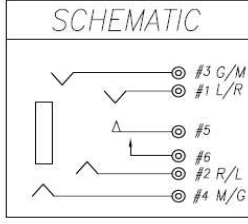
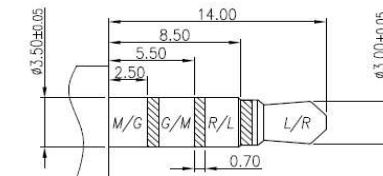


Int. Speaker

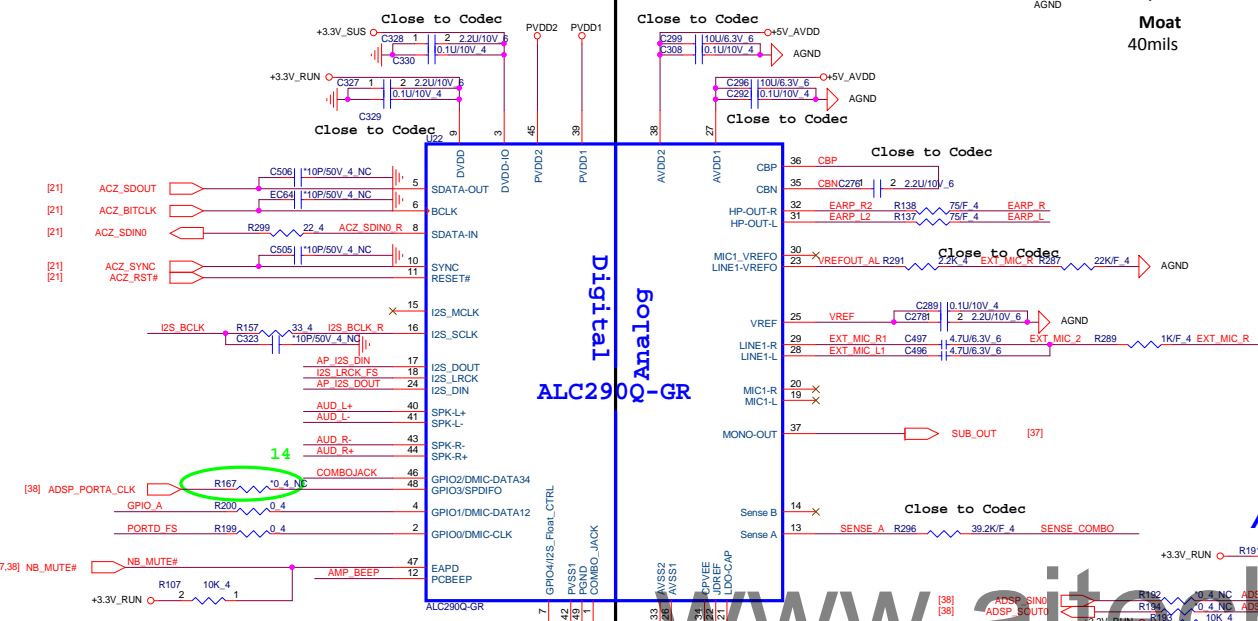
AUD R+ R	L10	TH160808U600	AUD R+ R	4
AUD R- R	L11	TH160808U600	AUD R- R	3
AUD L- L	L12	TH160808U600	AUD L- L	2
AUD L+ R	L13	TH160808U600	AUD L+ R	1

JSPK1

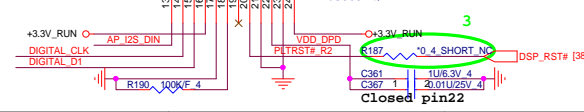
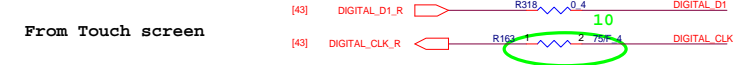
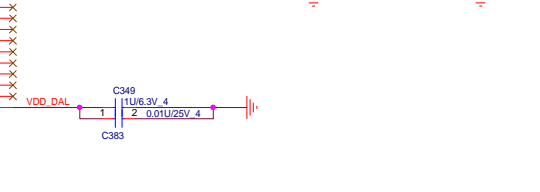
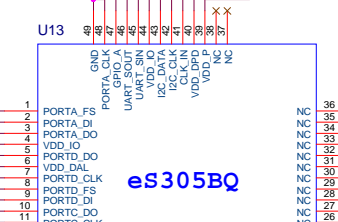
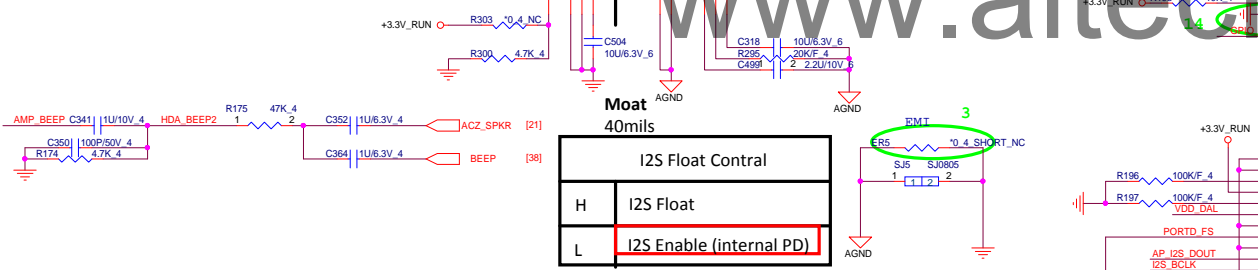
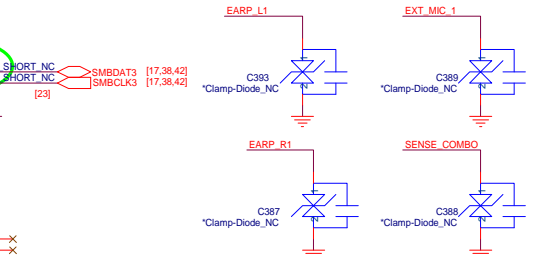
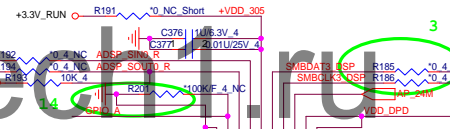
Audio Combo Jack



Audio Jack type:
Normal Open
Combo Jack (IPHONE)



Audio Processor



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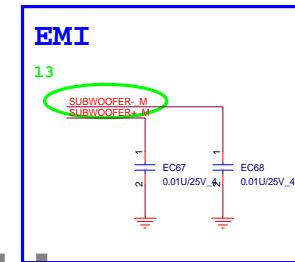
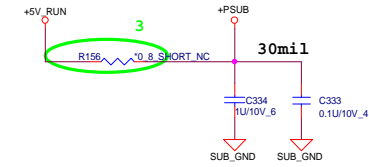
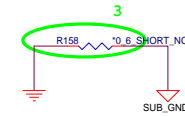
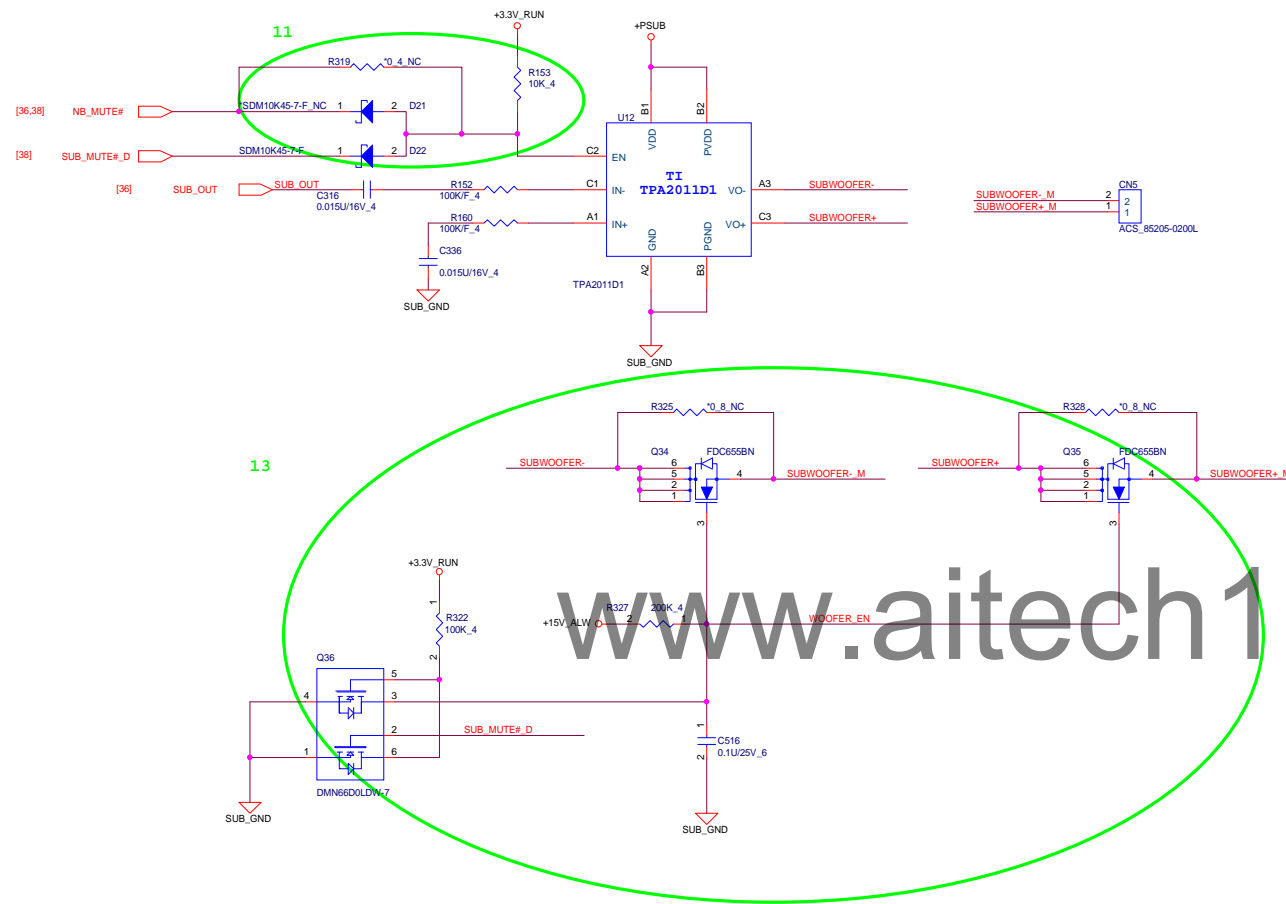
PROJECT : JWA

Size Document Number **CODEC (CX20672)** Rev 3A

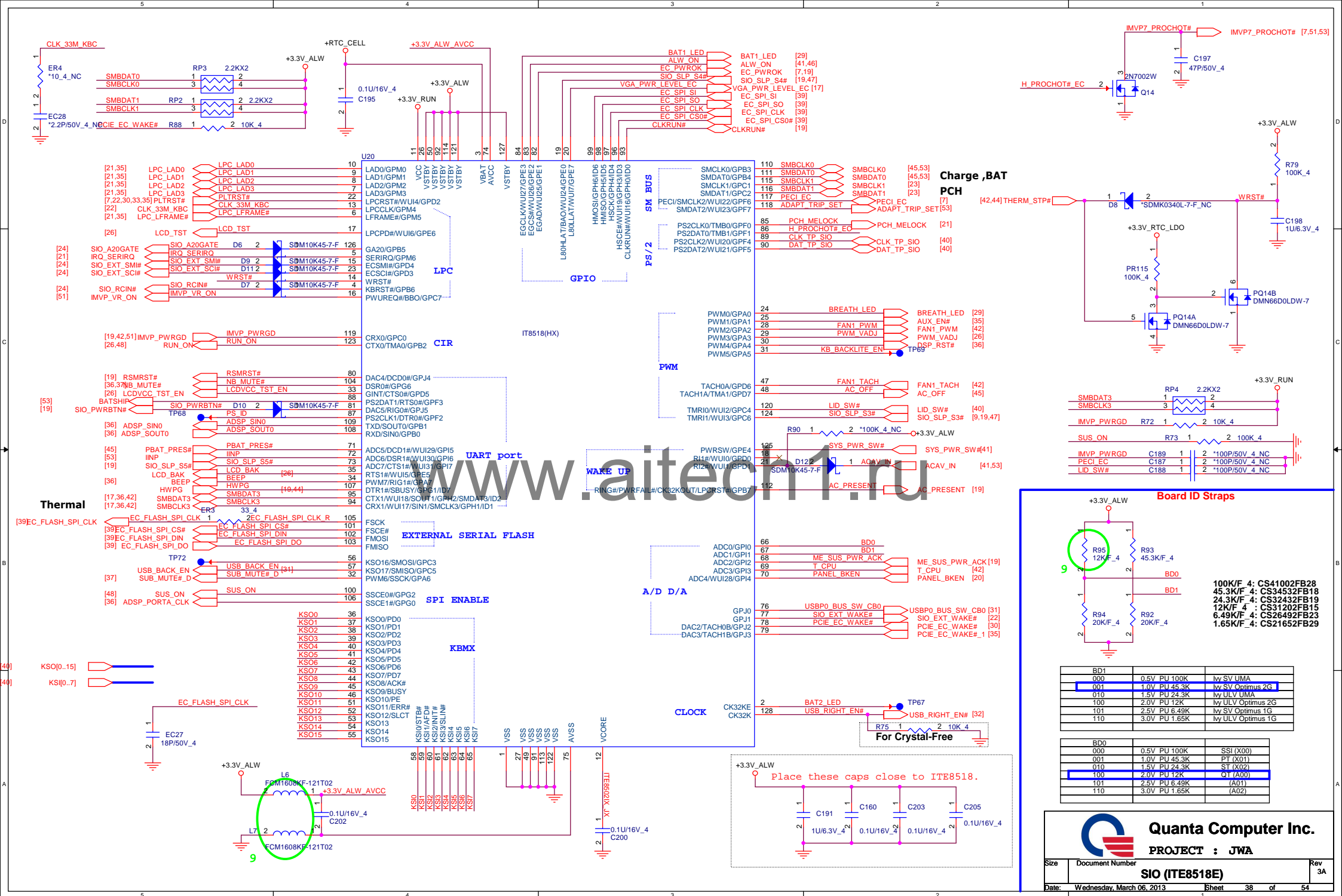
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Subwoofer Amp

Follow JW9

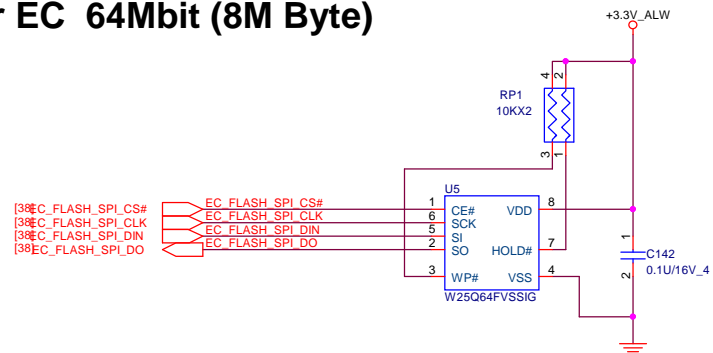


	R319	D21	D22	R153
NB_MUTE control SUB.	X	X	X	O
SUB can be controlled separately.	O	X	O	X

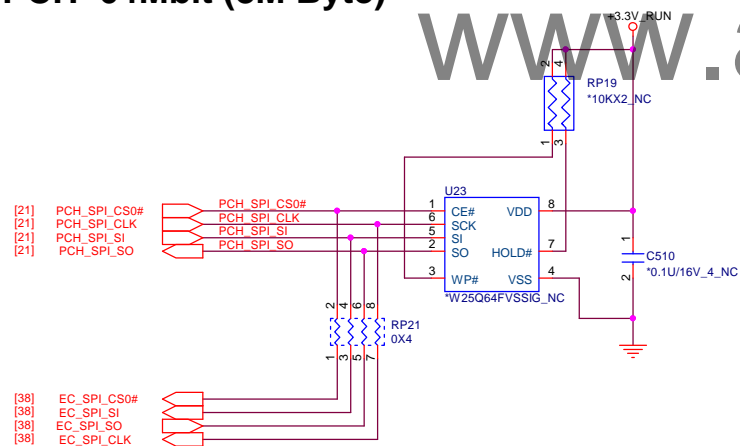


FLASH / RTC

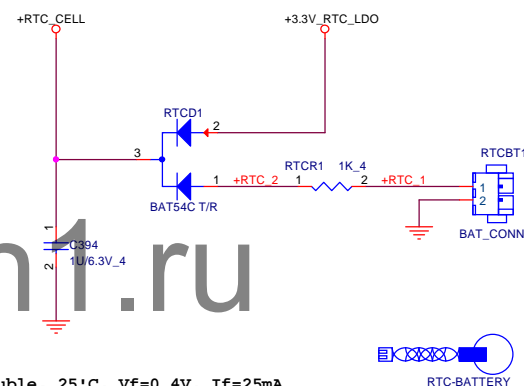
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)



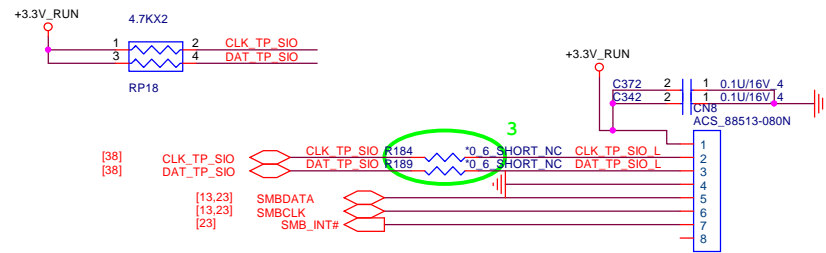
RTC



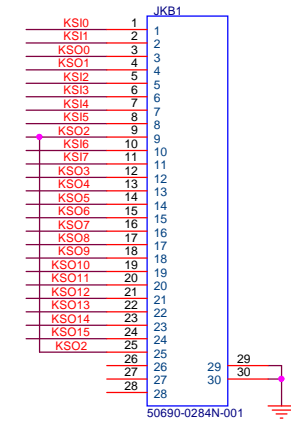
Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA



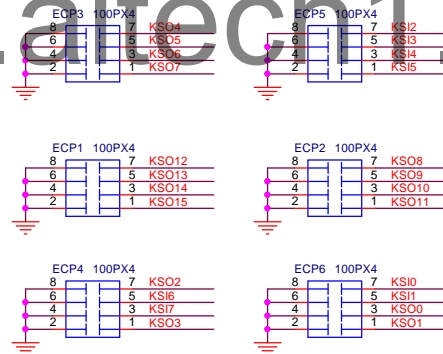
TP CONNECTOR



KB CONN

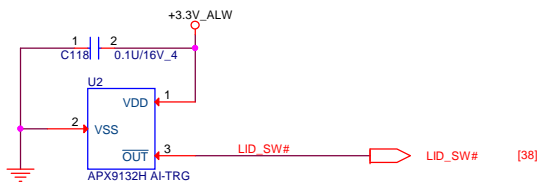


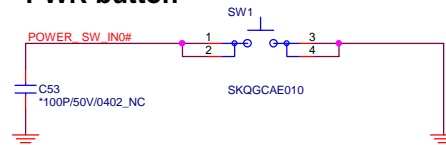
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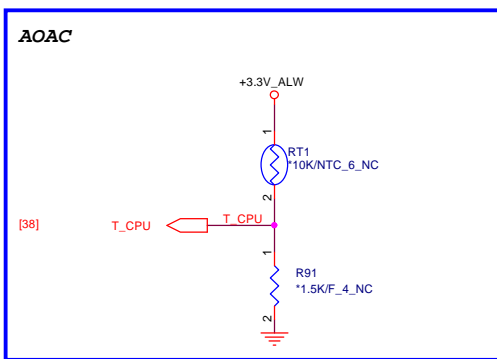


Layout Note: 100P CAPS CLOSE TO JKB1

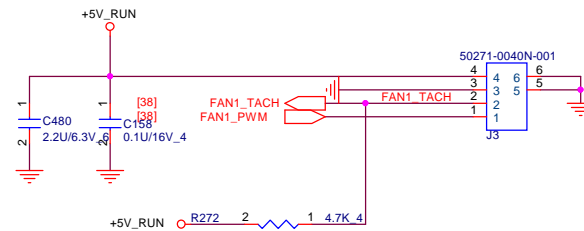
HALL Sensor





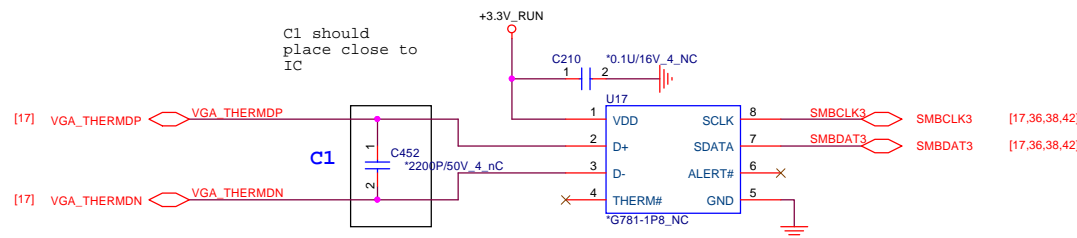


FAN CONN



G781-1P8

SMBus address is 1001101xb (9Ah) (x is R/W bit).

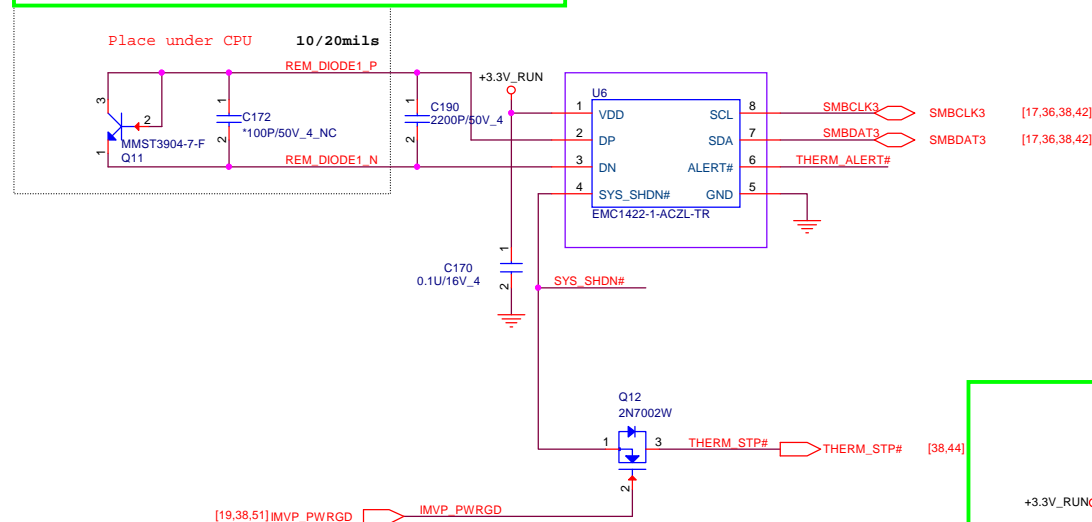


EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77°C	83°C	89°C	95°C	101°C	107°C
6.8K	78°C	84°C	90°C	96°C	102°C	108°C
10K	79°C	85°C	91°C	97°C	103°C	109°C
15K	80°C	86°C	92°C	98°C	104°C	110°C
22K	81°C	87°C	93°C	99°C	105°C	111°C
33K	82°C	88°C	94°C	100°C	106°C	112°C

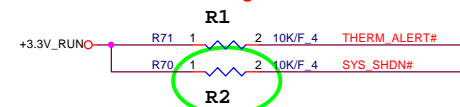
THERMAL IC

- Place C586 close to EMC1422-U1
 - Place C585 to be close to Q38
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C586, then C585 should be dummy



CHECK OTP WITH Thermal.

OTP 85 degree C



EMC1422
OTP 85 degree : R1 = 10K, R2 = 6.8K
OTP 90 degree : R1 = 6.8K, R2 = 10K
OTP 90 degree : R1 = 10K, R2 = 10K

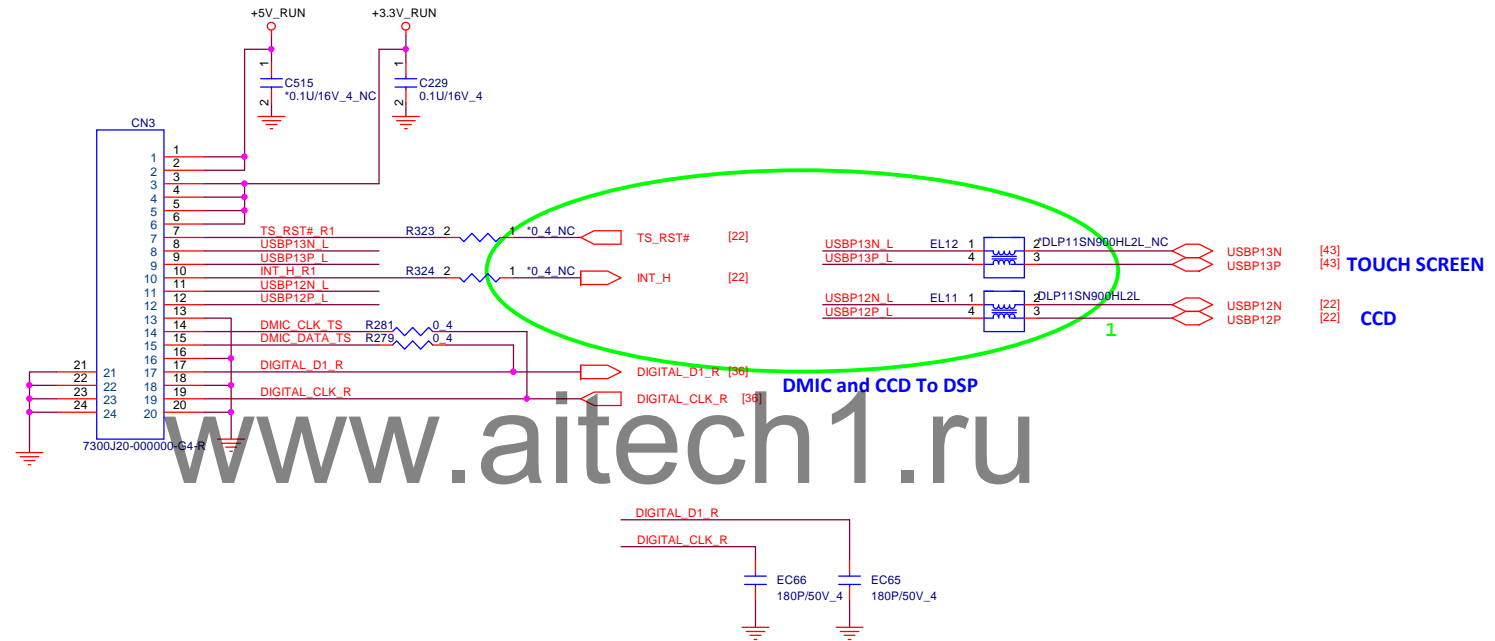
NTC7718W
OTP 85 degree : R361 = 18.7K, R362 = 2K
OTP 91 degree : R361 = 10.5K, R362 = 7.5K



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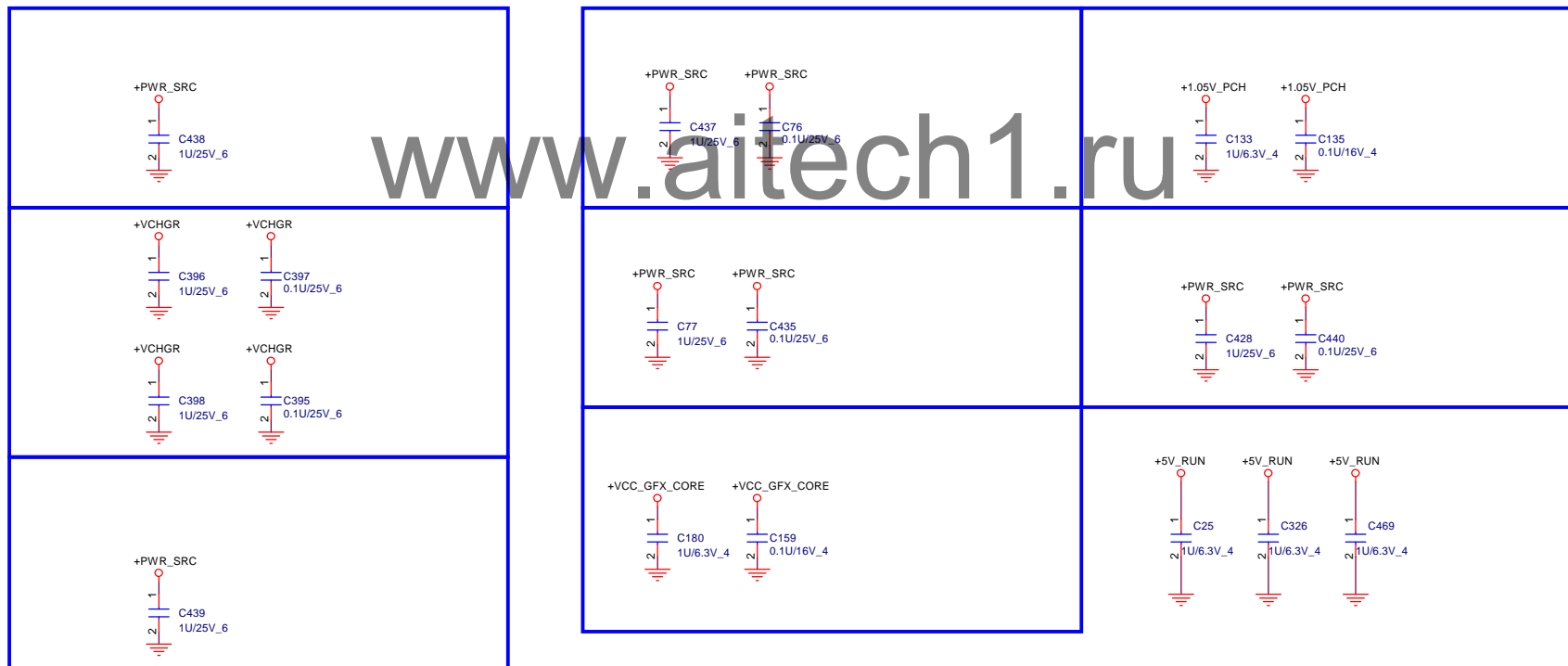
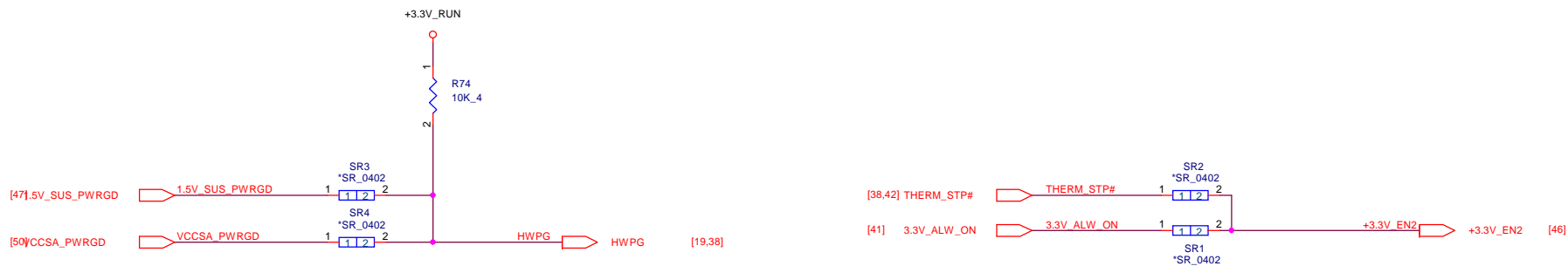
Touch Screen

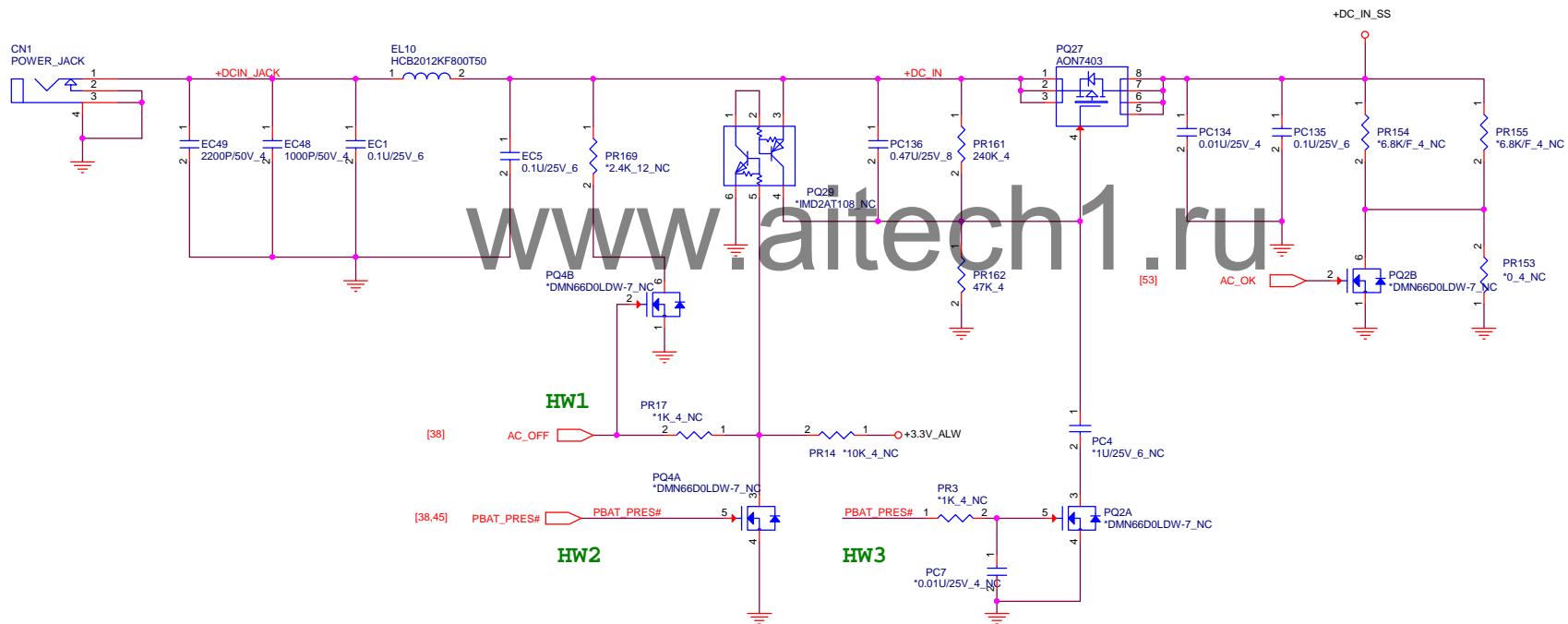
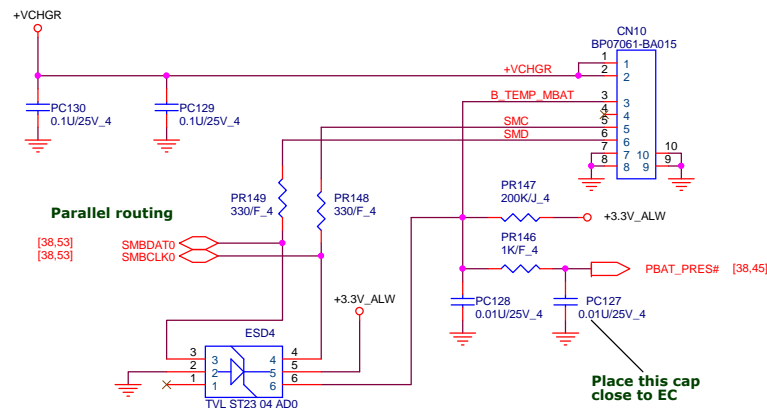


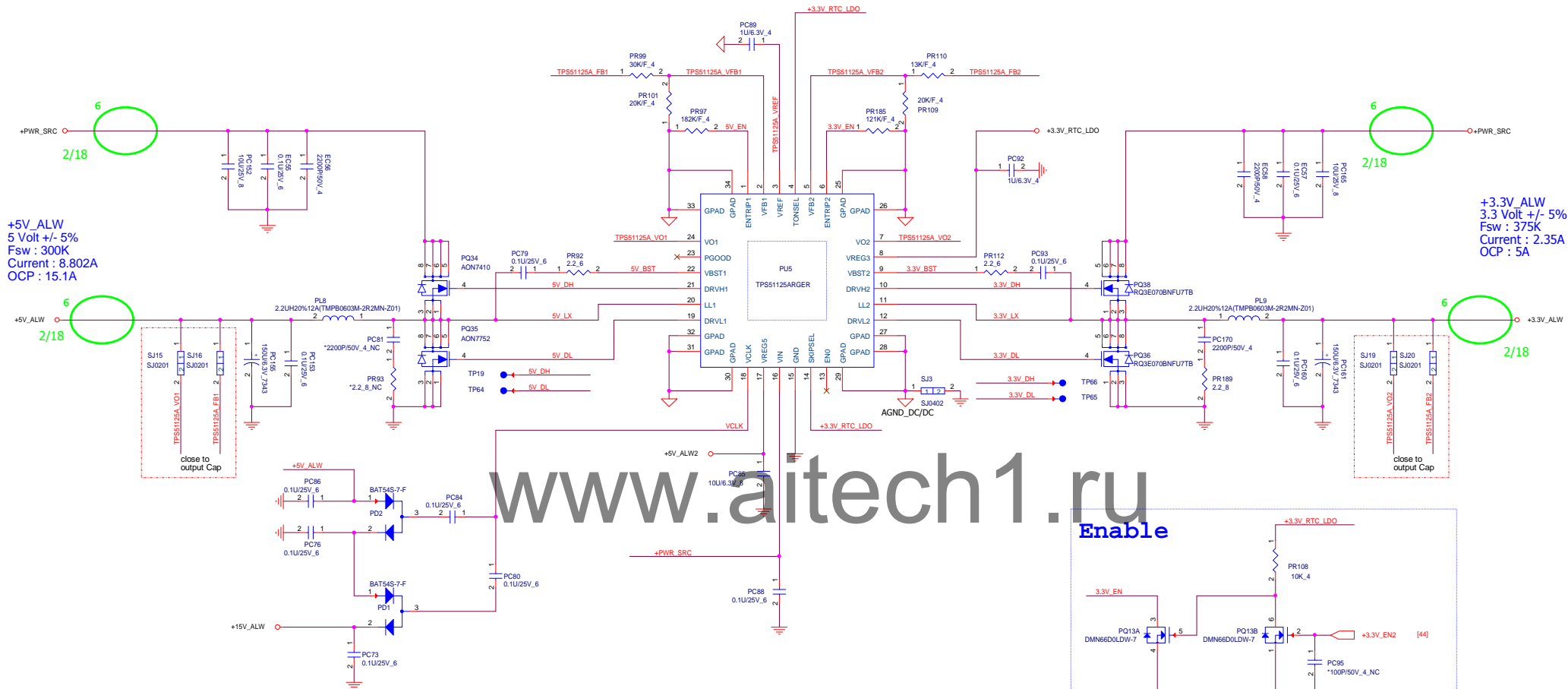
Quanta Computer Inc.

PROJECT : JWA

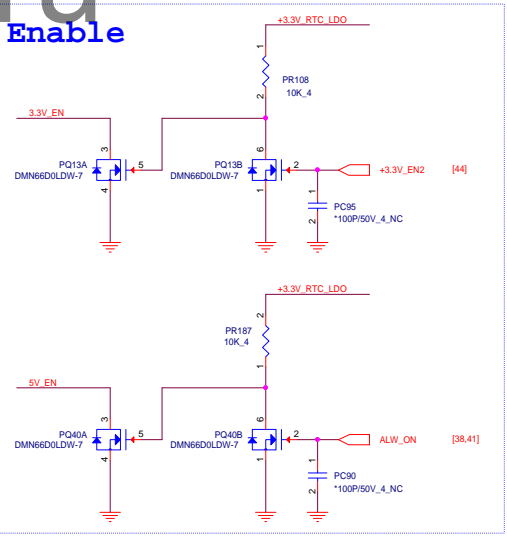
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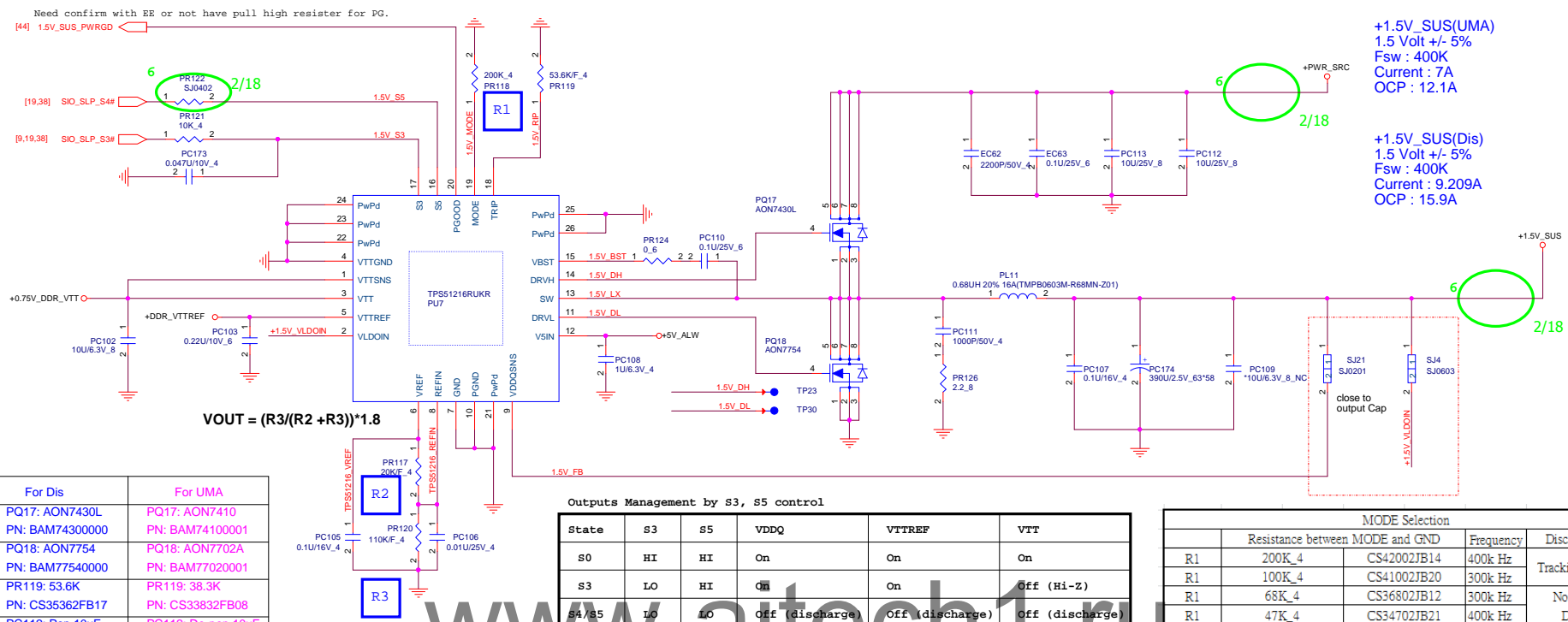






TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz



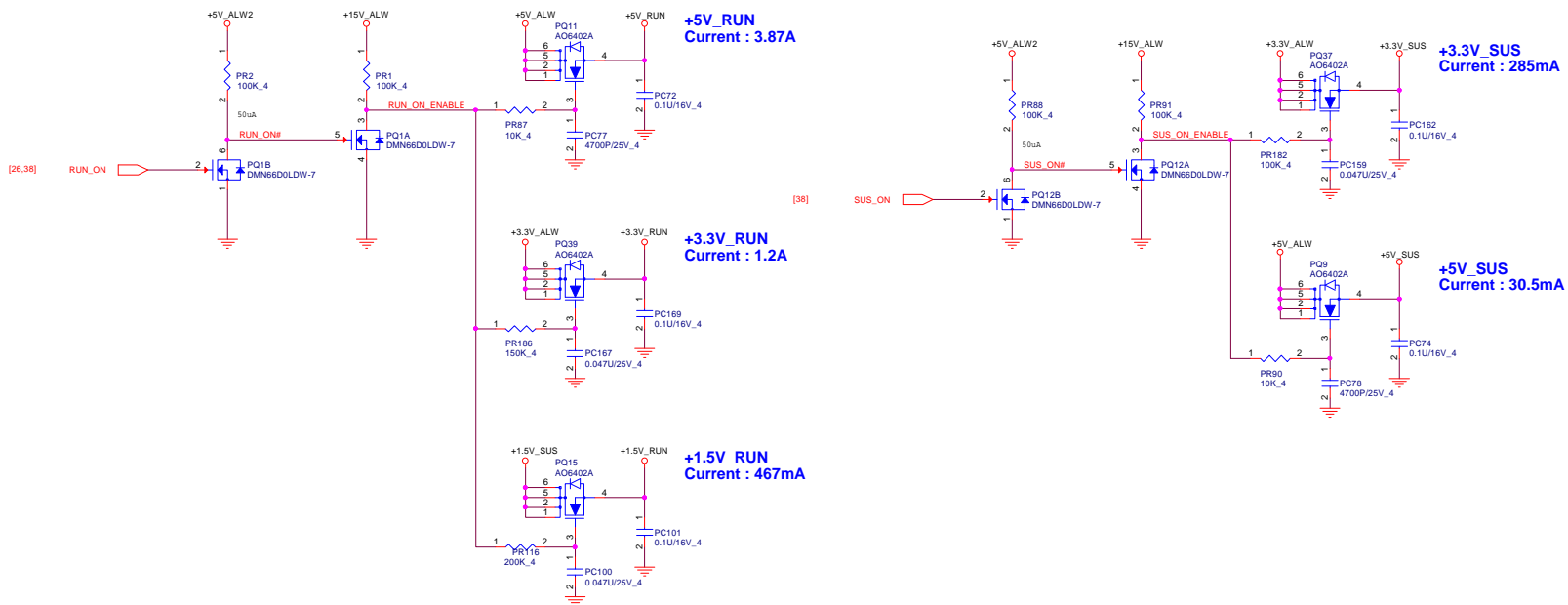


For Dis	For UMA
PQ17: AON7430L PN: BAM74300000	PQ17: AON7410 PN: BAM74100001
PQ18: AON7754 PN: BAM77540000	PQ18: AON7702A PN: BAM77020001
PR119: 53.6K PN: CS35362FB17	PR119: 38.3K PN: CS35382FB08
PC112: Pop 10uF	PC112: De-pop 10uF

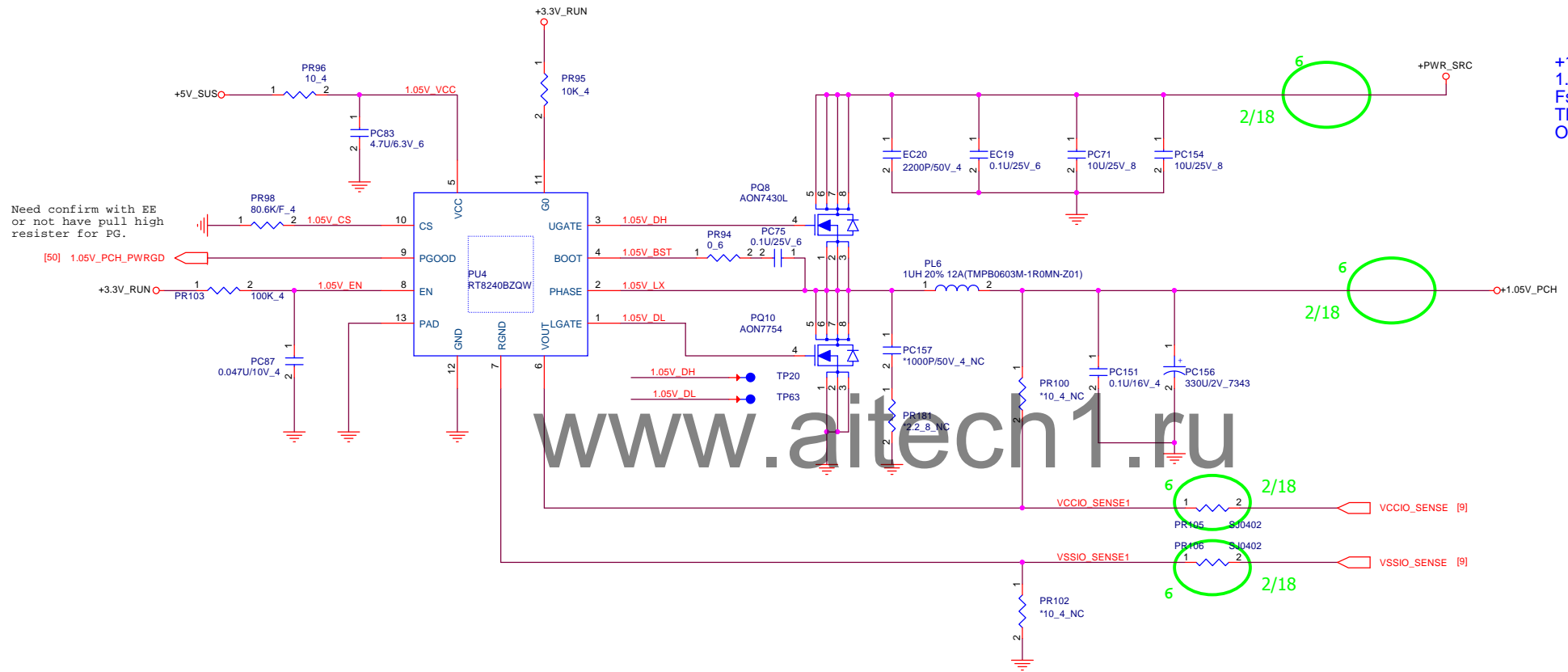
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

MODE Selection				
	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K ₄	CS42002JB14	400k Hz	Tracking Discharge
R1	100K ₄	CS41002JB20	300k Hz	
R1	68K ₄	CS36802JB12	300k Hz	Non-tracking Discharge
R1	47K ₄	CS34702JB21	400k Hz	



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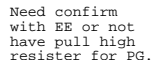
+1.05V_PCH
1.05 Volt DC +/- 2%
Fsw : 400K
TDC : 11.606A
OCP : 20A



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	+1.05V_PCH / VTT (RT8240BZQW)	1A
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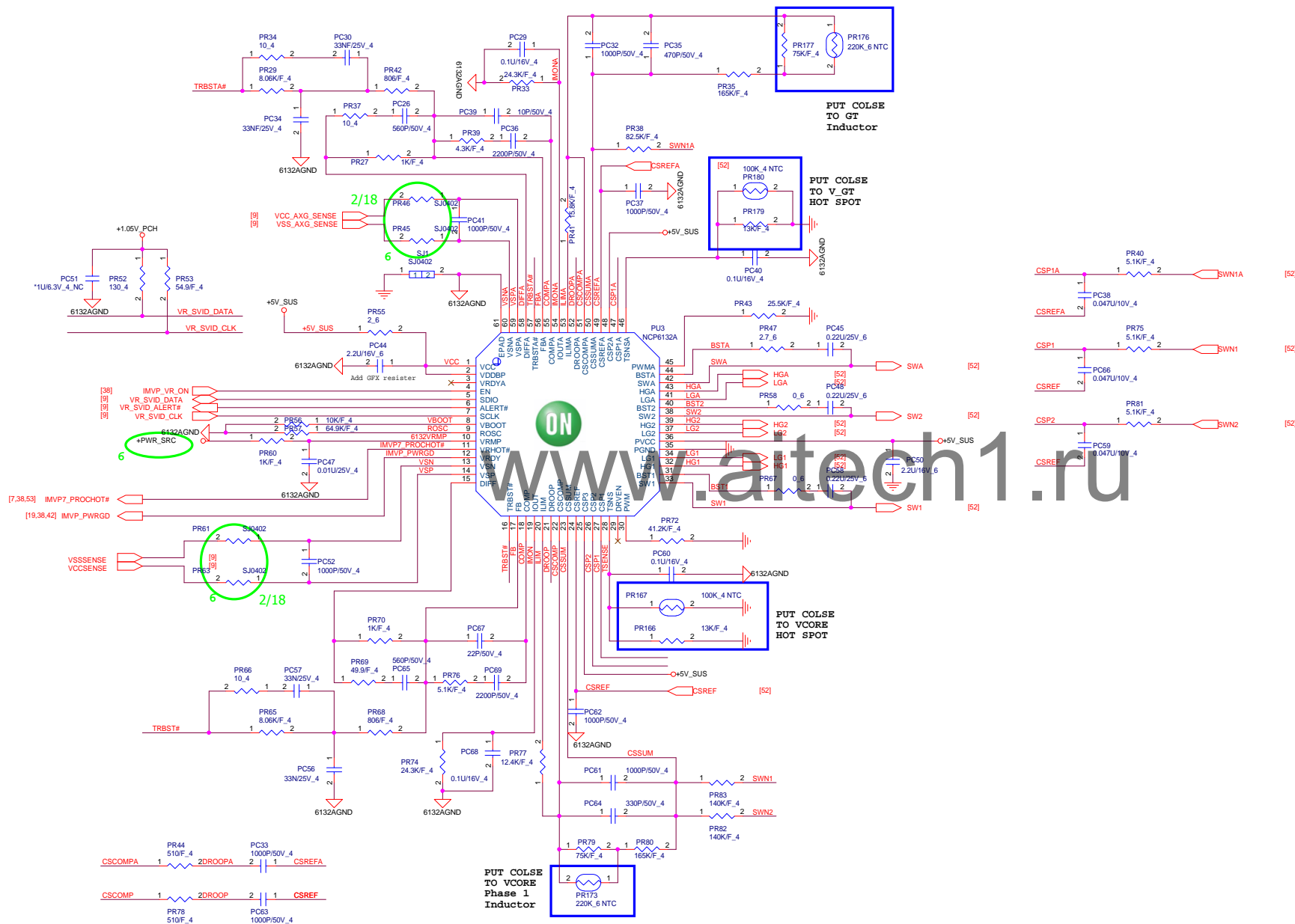


VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V

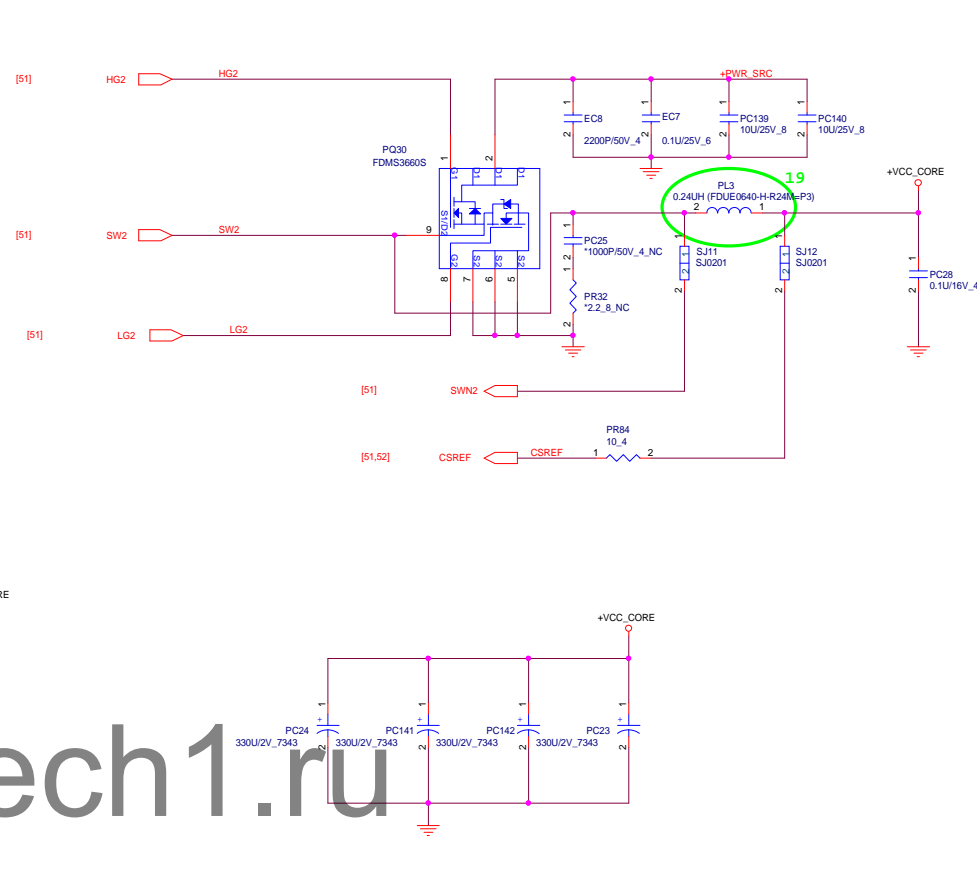
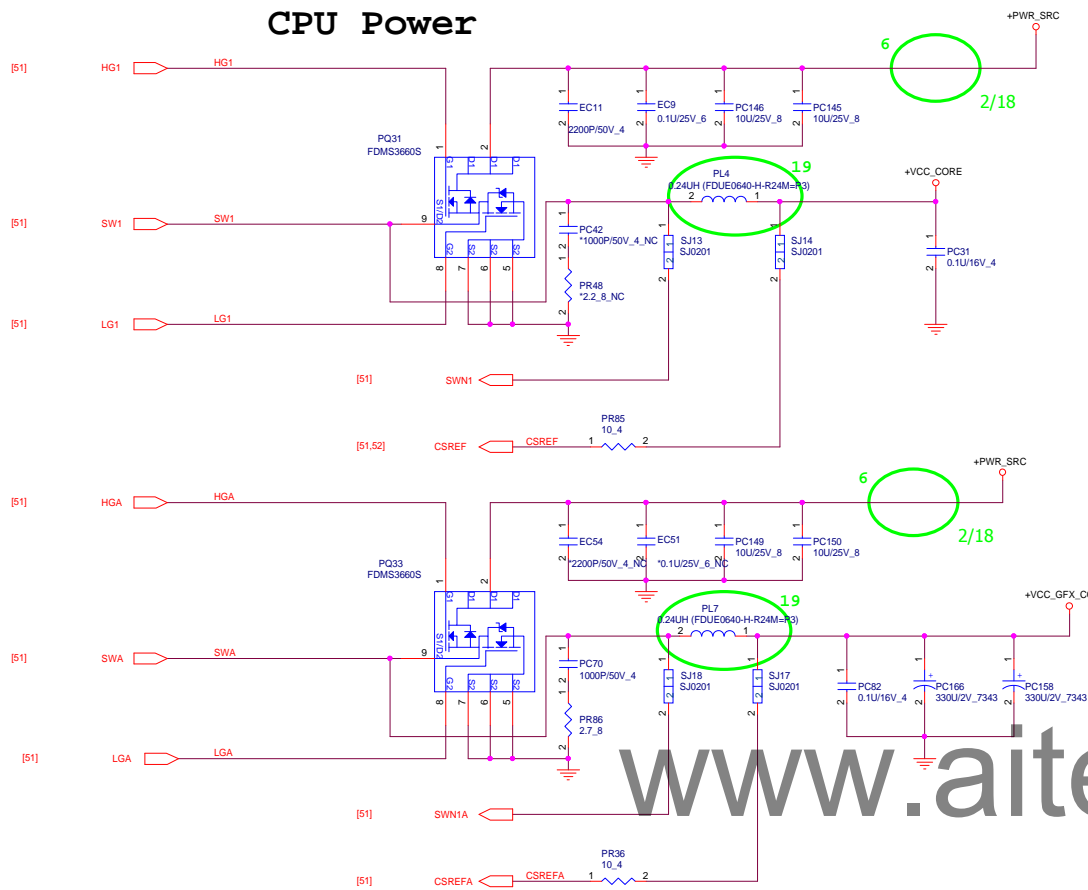




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CPU Power



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